

5-1-2002

Chip-package co-design of a low voltage operational transconductance amplifier

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Chip-Package Co-Design of a Low Voltage Operational Transconductance Amplifier

by

Prachi Kulkarni

A Thesis Submitted
in
Partial Fulfillment
of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electrical Engineering

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ROCHESTER, NEW YORK
MAY 2002

Title of thesis: Chip-Package Co-Design of a Low Voltage Operational
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Acknowledgement

This thesis was required as one of the requirements for graduation for the Master of Science degree in Electrical Engineering by Rochester Institute of Technology.

First and foremost I would like to take this opportunity to show my appreciation to my advisor Dr. P.R.Mukund, whose help, suggestions and encouragement helped me in all times of research and developing this thesis.

Also, I would like to express my gratitude to my parents Mr. Shripad kulkarni and Mrs. Anuradha Kulkarni for their undivided support towards my research and studies at Rochester Institute of Technology. I would like to show my deep indebtedness to Mayur Jagtap for his patience and support.

The research was supported by the Electrical Engineering department of Rochester Institute of Technology. I would like to take this opportunity to thank Dr. R. Unnikrishnan, Dr. S.Madhu and Dr. R. Bowman and Dr. S.Ramanan for their support.

I would also like to thank Harikrishna Parthasarathy and Sharmila Sridharan for helping me write my thesis. Finally, I would like to thank Sri Priya Bandi Rachaih for her layout, which was used in my thesis.

Abstract

The concept of chip package co-design is novel. The chip-package interaction for a low voltage operational transconductance amplifier (OTA) is described in this thesis. The effects on the stability of the OTA were studied when the compensation capacitor is placed in the package instead of on the chip. As the packages have become more sophisticated, it is possible to enhance the operation of the chip-package co-design. A detailed theoretical analysis of the transfer function of the OTA is given. Stability issues like the phase margin and the unity gain bandwidth frequency are discussed. A comparison of the specifications is made between compensation capacitor (C_c) on-chip and C_c on package.

The other part of the thesis discusses the effects of power supply noise on the op-amp. As the technology has encouraged the scaling of the feature size more number of functional blocks can be placed on the chip. As a result of this the density of integrated circuits has increased to a great extent. Due to the switching of the digital gates, current distributed in the power distribution planes can cause noise in the power supply of the op-amp. Thus this may lead to unwanted noise in the power distribution system. The effect of the power supply noise on the op-amp is also analyzed in the thesis.

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Chapter 1

Introduction

1.1 Application

The operational amplifier (op-amp) is one of the most important building blocks in analog signal processing. The op-amp provides very high input impedance and therefore provides good isolation. The output current, voltage and power can also be increased in order to suit the applications. These qualities of the op-amp are utilized in circuits like integrators, differentiators, buffers, Analog-to-Digital Converters and Digital-to-Analog converters.

The amplifier's performance usually limits the operating frequency of the application because the gain rolls off as the system frequency increases. Due to the shrinking of the power levels, the dynamic range of the overall circuit is reduced, as a result of which the signal handling capability is also limited. The noise sensitivity of the op-amp is also a critical parameter to be considered as far as the overall system is concerned [7]. Without a thorough understanding of the operation and the basic limitations of these amplifiers, the circuit designer cannot determine the actual response of the overall system [15].

Op-amps have a wide range of applications owing to their performance as mentioned before. One of the important applications is discussed in the following sub-section.

Sample and Hold Circuit

The purpose of the sample and hold is to track and hold the analog input signal for sufficient time so that the Analog-to-Digital converter completes its conversion. The sample and hold circuit serves as an interface between the input analog signal to be encoded and the rest of the ADC [11]. Figure 1.1 shows a sample and hold circuit where the op-amp is used.

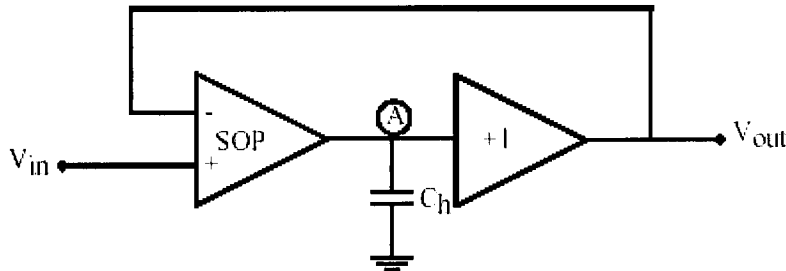


Figure 1.1 Switched op-amp sample and hold circuit [7]

The sample and hold (S/H) circuit is typically a pair of voltage follower op-amps in an open loop or closed-loop configuration linked by a holding capacitor. The S/H circuit is used for data conversion applications. The switched op-amp

(SOP) shown in figure 1.1 has high output impedance when it is shut off. During the hold mode the SOP is switched off and the capacitor charges to the sample voltage and then holds this voltage. The output buffer provides the voltage sampled on the capacitor at the output.

1.2 Principle of Operational Transconductance Amplifier (OTA)

The working of the OTA can be explained using the following figure.

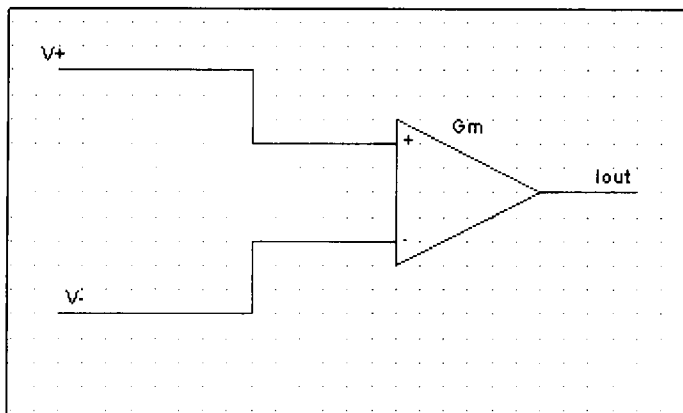


Figure 1.2 Principle of an OTA

The OTA converts the input voltage to an output current by means of the device transconductance. The transconductance g_m is defined as the ratio of the change in the drain current to the change in the gate to source voltage.

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}, const} \quad (1.1)$$

The transconductance also depends on the transistor size and the drain current [1] and is given by,

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (1.2)$$

where C_{ox} is the oxide thickness, W is the width of the transistor, L is the length of the transistor and I_D is the drain current.

Various techniques have been realized using CMOS devices for designing OTA's. The design of OTA's continues to develop as the transistor channel lengths and the supply voltage scale down with each new generation of CMOS technologies. In this thesis, a low voltage operational transconductance amplifier has been designed and has been used for the analysis.

1.3 Thesis outline

The thesis is basically divided into two parts. The first part explains the stability of the op-amp when the compensation capacitor is placed on the package. The second part elaborates on the power supply noise and its effect on the characteristics of the op-amp.

The compensation capacitor (C_c), which is used to move the dominant pole to a low frequency, and the other poles and the zeros beyond the unity gain bandwidth frequency, occupies almost one-third of the chip area. In order to optimize the design to reduce the chip area, the compensation capacitor can be moved to the package. So it is important to study the effects of parasitics by moving the capacitor off chip. This is the main focus of chip-package co-design.

When the C_c is placed on the board, the stability of the op-amp becomes an issue. The parasitic components will be added on either side of the capacitor nodes. Thus, a π network of resistors, inductors and capacitors will be formed. Even though packages have become more sophisticated resulting in reduced parasitics, it is still important to study the stability issues.

The theoretical analysis of the transfer function between the output and input of the small signal model of the op-amp with the parasitic components is explained. A comparison of the stability of the amplifier is done when the compensation capacitor is on the chip and when it is in the package. The simulation results are given to support the theoretical results.

The second part of the analysis done on the op-amp is to study its sensitivity to noise on the power supply. A theory has been formulated to determine the output noise voltage caused due to the power supply noise. The simulation results supports the theoretical results.

1.4 Organization

The low voltage two-stage operational transconductance amplifier is explained in chapter 2. The design of a two-stage transconductance amplifier is also presented. The advantages and the constraints of low voltage design are discussed.

Chapter 3 contains the theoretical analysis of the transfer function of the two-stage OTA when the compensation capacitor is placed on the board. It explains the small signal model of the two-stage op-amp with C_c on the package. Simulation results are also presented. A detailed study of the frequency response of the system is done. It also contains the simulation results like the slew rate, open loop gain plot.

The concept of noise on the power supply is explained in chapter 4. The chapter deals with the theoretical analysis of the noise on the power supply and its effect on the op-amp. A comparison is made between the theoretical analysis and the simulated results.

Finally in Chapter 5, the thesis is summarized and directions for future work are discussed.

Chapter 2

Background

2.1 Low Voltage Design and its Limitations

CMOS op-amps were typically designed to operate at large supply voltage, that is $\pm 5\text{V}$ or larger. The supply voltages for digital circuits have reduced in order to minimize power consumption. As a result, it is necessary to design amplifiers at lower supply voltages to be compatible with digital circuits in mixed-signal systems.

The current handling capability of the MOS transistors is limited at low supply voltages unless extremely large W/L ratios are used. But this results in consumption of large die area and low bandwidth due to the large gate-source capacitance [10].

The transistors operate in the inversion mode when smaller drain current is present because of the small gate voltage. As the drain current increases the transistor goes into saturation mode. In the saturation region the characteristic of the transistor is in first order and is described by a quadratic relation.

The gate-source voltage is given by,

$$V_{GS} = \sqrt{\frac{2LI_D}{C_{ox}W\mu}} + V_{Th} \quad (2.1)$$

where V_{Th} is the threshold voltage, I_D the drain current, μ the mobility of the charge carriers, C_{ox} the oxide capacitance, W the width of the transistor and L is the length of the transistor.

Due to the square root relationship a relatively large gate-source voltage is required to handle large drain currents. Normally to provide high gain, the transistors have to be in saturation. To achieve this, the drain-source voltage should be greater than the difference of the gate-source voltage and the threshold voltage.

As the supply voltage decreases, the ability to stack transistors and still keep them all in saturation becomes increasingly difficult. In order to overcome the limitation imposed by the reduced power levels, a high gain stage can be added to the differential stage. In CMOS technology two stages are sufficient in order to improve the gain of the single stage. Depending on the process and the available supply voltage, different strategies are found, like adopting a cascode or folded cascode topology to achieve high gain. In this thesis the operational transconductance amplifier has been implemented in a standard $0.25\mu\text{m}$ CMOS process with a supply voltage of $\pm 2.5\text{V}$.

2.2 Circuit Description

The basic block diagram of a two-stage operational amplifier is shown in figure 2.1. It comprises three sections: a differential gain stage, a high gain stage and biasing circuitry [2]. The description of the different stages is provided in the following sub sections.

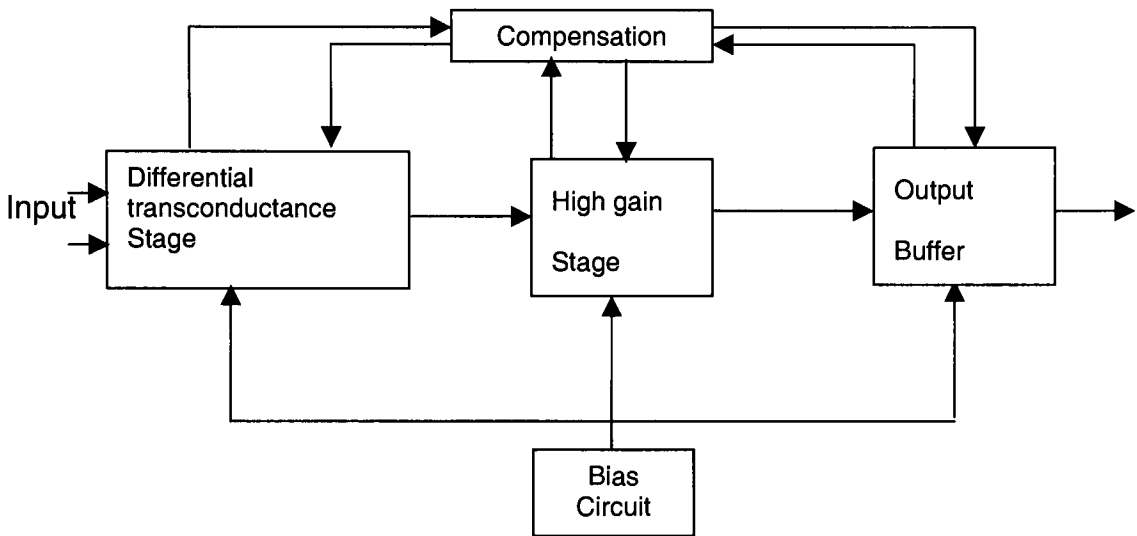


Figure 2.1 Block Diagram of a Two-stage Op-amp

2.2.1 Differential Stage

Digital circuitry generates a large amount of switching noise, which appears in the common substrate. This noise is also coupled to the transistors through the parasitic capacitances. Also noise may be present at the input. It is therefore necessary to take precautions in order to make the analog circuit highly

immune to this noise coupling. Differential circuitry is a technique, which provides a way to achieve this immunity. The input transistors in the differential stage cancel out the effect of this noise coupling.

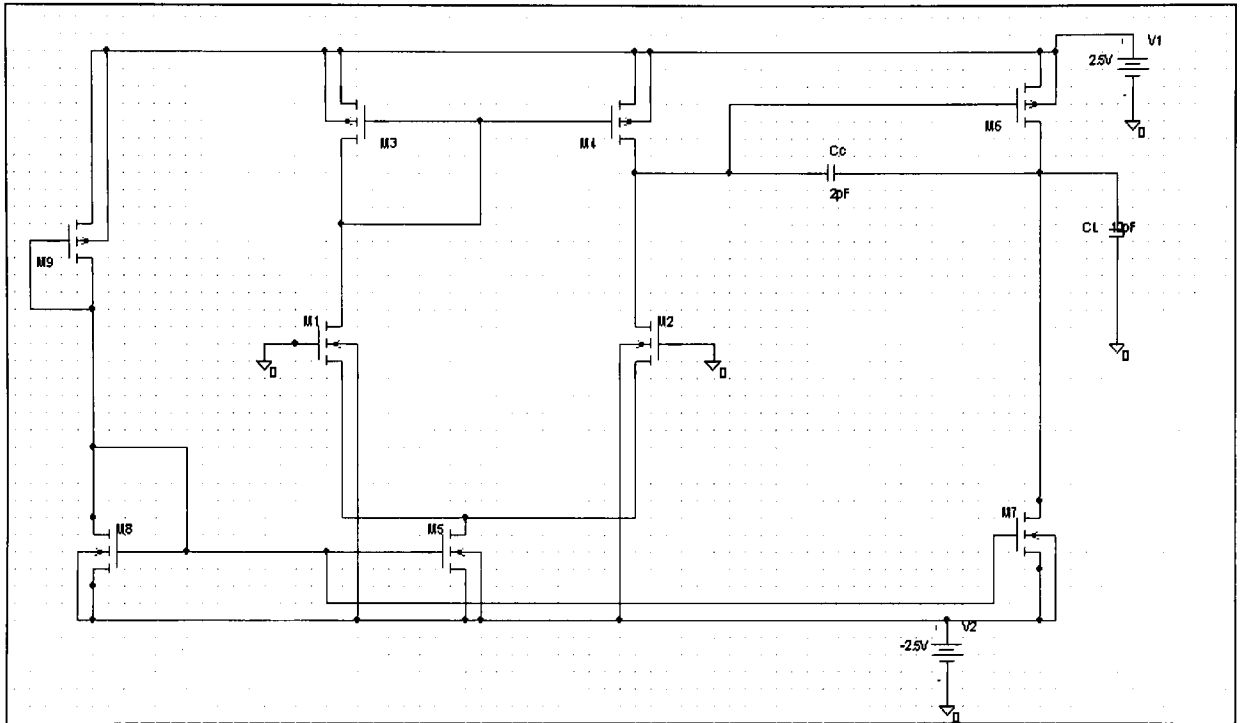


Figure 2.2 Schematic of a Two-stage Operational Transconductance Amplifier

The figure 2.2 shows the basic configuration of the two-stage operational transconductance amplifier. Transistors M1- M5 forms the differential stage. The objective of the differential amplifier is to amplify the difference between the gate voltages of M1 and M2. The gate of transistor M1 is the inverting input and the gate of transistor M2 is the non-inverting input.

The gain of the differential stage is the product of the transconductance of M2 and the effective output resistance at the drain of M2 i.e. the combination of the output resistance of transistor M2 and the output resistance of the active load, transistor M4.

When the differential stage is balanced, under DC operating conditions, the transistors M1 through M4 have a drain current equal to half of the tail current. Transistors M3 and M4 are the active load devices. The active load devices have the following advantages:

1. The use of active load devices creates a large output resistance.
2. The current mirror topology performs the differential to single-ended conversion of the input signal.

The DC currents of each transistor are listed in the table shown below

Transistor No	1	2	3	4	5	6	7	8	9
I_d (current in μA)	$3\mu A$	$3\mu A$	$3\mu A$	$3\mu A$	$6\mu A$	$60\mu A$	$60\mu A$	$24\mu A$	$24\mu A$

Table 2.1 DC Currents of each transistor in the op-amp

The biasing circuitry is designed such that it provides a bias current of $24\mu\text{A}$. Transistors M8 and M5 act as the current mirror transistors as their gate and source are at the same potential. Thus, the tail current in transistor M5 depends upon the ratio of the size of transistors M8 and M5. The output stage is designed such that its drain current is ten times that of the tail current.

2.2.2 Output Stage

The purpose of the second stage is to provide additional gain to the amplifier. It consists of transistors M6 and M7. The input to the second stage is the output from the drain of the transistor M4. Transistor M6 has a common source configuration. Thus the transistor M7 acts as an active load. These two transistors offer a very high output resistance, which is essential for high gain. In order for the circuit to work properly, both the transistors must be operating in the saturation region.

Since high signal levels are likely to occur, the output stage should be able to deal with high voltages and high currents. The output stage also determines the signal handling capability of the op-amp, which is determined by the dynamic range. Also the output stage has to cope with the load connected to the output terminal. Very low resistive loads require a maximum output current. The

capacitive load on the other hand, determines the minimum current that is needed to obtain sufficient phase margin and stability.

2.2.3 Compensation Technique

To maintain stability in a two-stage amplifier, some form of compensation must be applied inside the feedback loop. To achieve this, a capacitor is added in the loop to create a dominant pole at a very low frequency. So a standard Miller compensation is used, which places a pole splitting capacitor between the output of the first stage and the output of the second stage. This has the effect of creating a dominant low frequency pole and moving the second pole to a higher frequency, which will ensure amplifier stability when it is placed in a feedback loop. This capacitor is called the Miller compensation capacitor. A rule of thumb is that the C_c should be at least 0.22 times the load capacitor, for a phase margin of 45 degrees [2]. After the compensation capacitor is added to the circuit the pole as well as the zeros of the amplifier shift.

The table shows the specifications based on which the design of the two-stage amplifier has been done. The open loop-gain of greater than 2500 is desired. The phase margin of 50° is specified for the system to be stable. The load capacitor of 10pF is specified, so the compensation capacitor value is approximately 2.2pF.

Supply Voltage	+/-2.5V
Open loop Gain	25000
Gain bandwidth	4MHz
Phase Margin	50°
Load (C _L)	10pF
Slew rate	3V/μS

Table 2.2 Specifications of the op-amp

2.3 Previous Work

The chip-package co-design is a novel idea, which studies the package issues that affect the chip design. A lot of work has been done in low voltage amplifier design and the constraints of low voltage. But no work has been done in the chip-package co-design area. There are various circuit configurations that have been studied to cope up with the low voltage constraint. The thesis emphasizes more on the chip-package interaction.

B. Ahuja had presented the mathematical analysis of the CMOS two-stage amplifier in terms of its frequency and noise characteristics. The technique described provides stable operation for a much larger range of capacitive loads and an improved power supply rejection ratio over a wide range of bandwidth [5].

Another critical aspect in low voltage design is the common-mode input swing, which depends on the input differential stage. G. Giustolisi explains the amplifier design for 1.2 V power supply. He adopts a folded mirror load in the input stage, which saves input swing, and includes a dynamically biased class-AB output stage providing both a rail-to-rail output swing and high output current [6].

Chapter 3

Chip Package Co-design

3.1 Stability of the OTA

The operational amplifier stability can be described in the frequency domain with the relationship between the phase margin and the open loop gain. The unity bandwidth of the operational amplifier is defined as the product of the open loop gain and the frequency at a point where the response of the amplifier is attenuating at a rate of -20dB/decade. Normally, the first pole of the amplifier occurs between 1Hz to 10KHz, and the second pole is at a much higher frequency, typically beyond the frequency where the open loop gain crosses the 0dB line [2].

The pole is defined as a point where the slope of the gain curve changes by -20dB/decade. Physically, the zero arises because the compensation capacitor provides a path for signals to propagate directly to the output. This occurs at high frequencies. Since there is no inversion in that signal path as there is in the operation at lower frequencies, stability is degraded.

The closed loop AC performance of a feedback circuit is dependent on the order of the denominator equation of the transfer function between the output

and the input of the op-amp. The order thus found is equivalent to the number of poles in the system.

Gain and phase margin are measures of stability for a feedback system. The larger the phase margin the more stable the system. The system stability conditions are checked using the bode plot, which plots the phase variation versus frequency. The standard Miller compensation scheme places a pole-splitting capacitor between the output of the overall amplifier and the output of the first stage of the amplifier [4].

A normal left half plane zero would add phase lead to improve stability but right half plane zero adds phase lag, which reduces stability. Also, by increasing the load capacitance the stability is reduced as the second pole moves to a lower frequency. A rule of thumb is that the zero and the second pole should be beyond the unity gain bandwidth product in order to achieve stability [3].

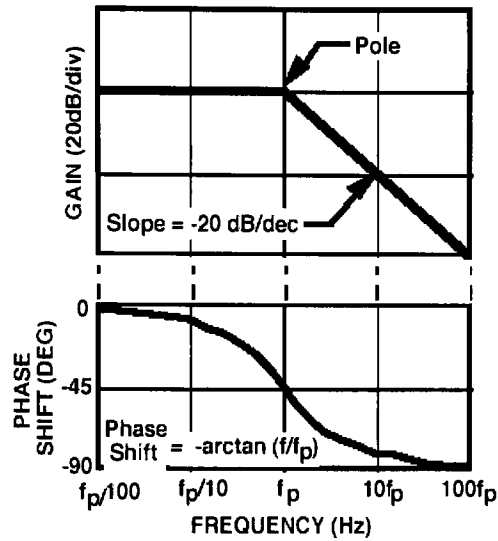


Figure 3.1 Bode plot [6]

Figure 3.1 shows the phase magnitude plot of a system. Bode plot computes the magnitude and phase of the frequency response of the system. The point where the slope starts changing by -20dB/decade indicates the presence of the first pole at that frequency. The point where the slope changes to $+20\text{dB/decade}$ indicates that a zero is present at that frequency. The unity gain bandwidth is equivalent to the amplifiers gain bandwidth product. The gain bandwidth of an op-amp is the frequency where the open loop gain crosses the 0dB line.

3.2 Frequency Compensation

Normally amplifiers are configured in negative feedback mode. The amplifier needs to be stable so that it will not oscillate for any value of resistive feedback applied. Thus, it is necessary to compensate the frequency performance of the amplifier to avoid oscillations in the closed loop response.

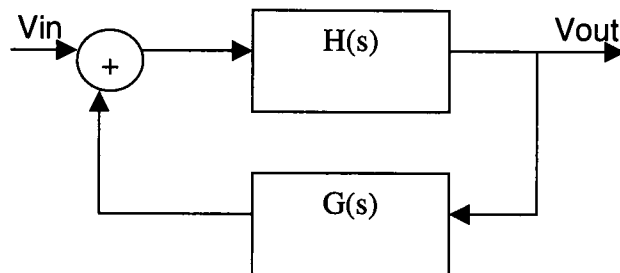


Figure 3.2 Feedback System

The frequency compensation of an amplifier means controlling its gain roll-off within a specific frequency band. At low frequencies, the gain-magnitude characteristics approach the dc open loop gain asymptotically. But as the frequency increases, the gain starts to roll off and crosses the 0dB axis at the unity gain frequency.

3.3 Simulation Results

The circuit was modeled in Affirma Analog environment tool using the TSMC 0.25 μ m technology. Appendix B lists the various process parameters used for TSMC 0.25 μ m technology process.

3.3.1 Slew rate

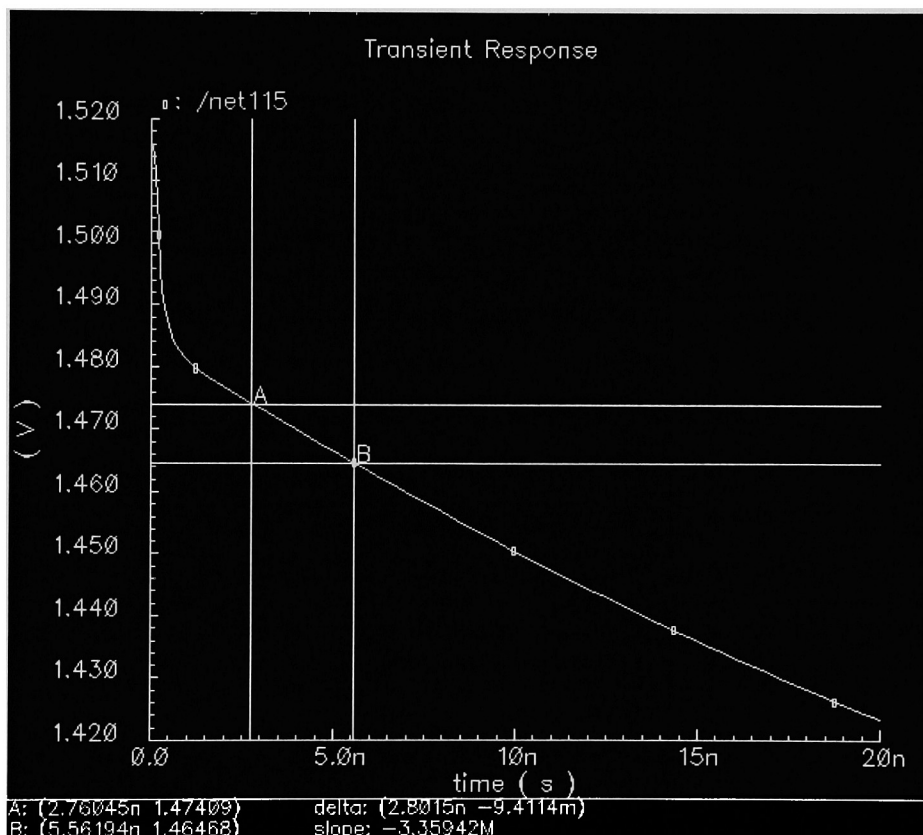


Figure 3.3 Slew rate plot

The maximum rate of change dV/dt is called the slew rate. The op-amp is connected in feedback and a pulse input is applied to its non-inverting

terminal and the output is plotted. The slew rate of the amplifier was observed to be $3.3 \text{ V}/\mu\text{s}$

2.3.2 Gain of the amplifier

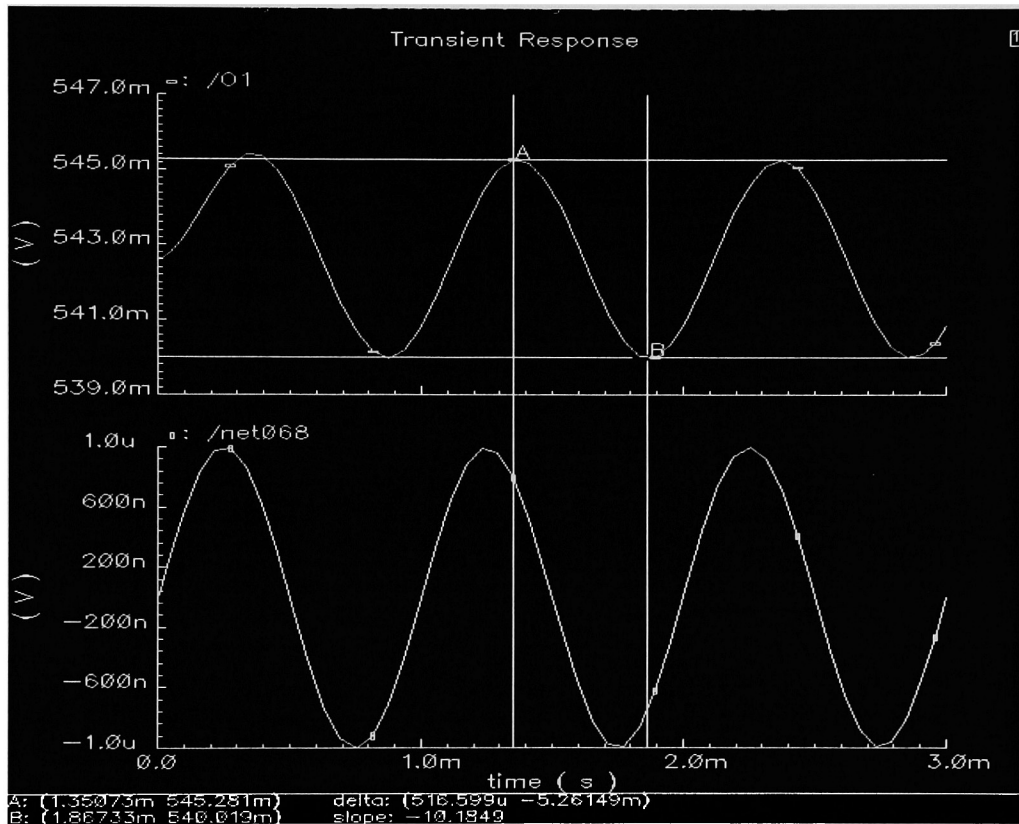


Figure 3.4 Gain Plot

Figure 3.4 shows gain of the op-amp obtained from simulation. The open loop gain of an amplifier is the ratio of change in output voltage signal to the change in differential input voltage. The inverting terminal is grounded and the input sine is applied to the non-inverting terminal with a specified amplitude and

frequency and the output is measured. The voltage gain was observed to be 2630 from the gain plot.

3.3.3 Frequency response of the amplifier

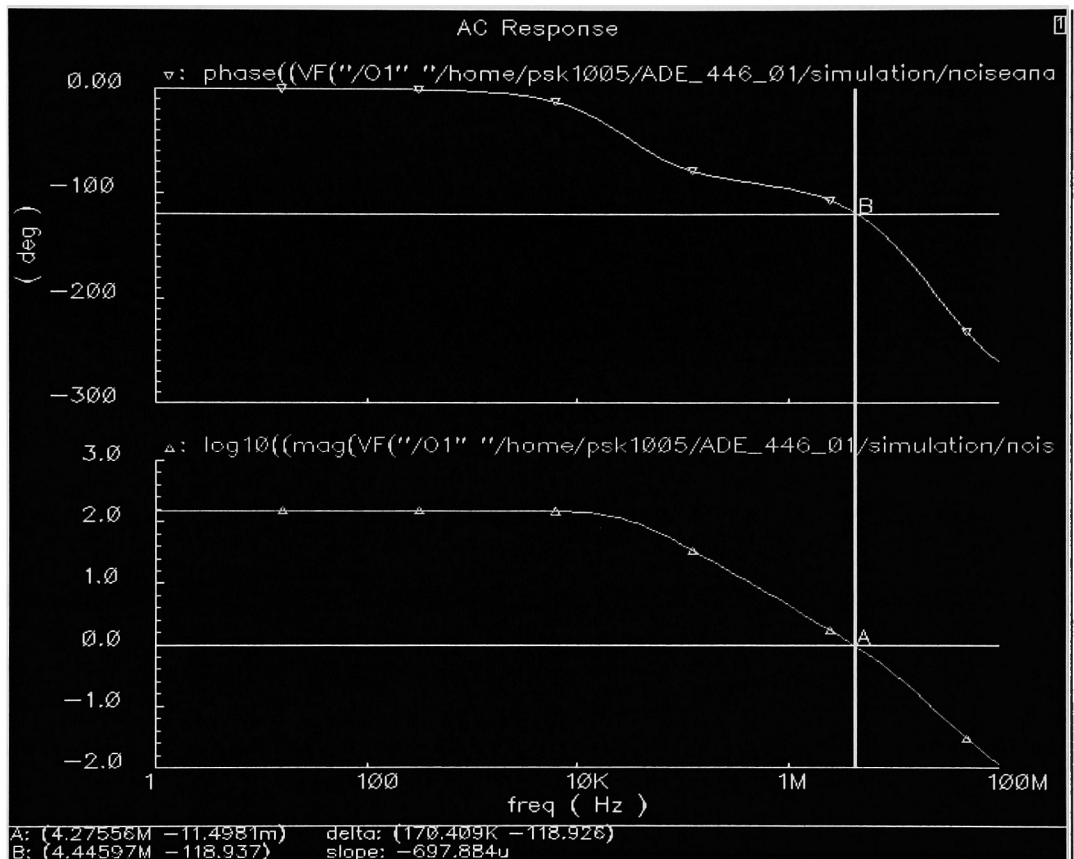


Figure 3.5 Magnitude-phase plot

Figure 3.5 shows the gain bandwidth frequency and the phase margin of the amplifier when C_c is on-chip. It is observed from the graph that the gain bandwidth frequency is 4.27MHz and the phase margin is 50°.

3.4 Small signal Model of the two- stage amplifier

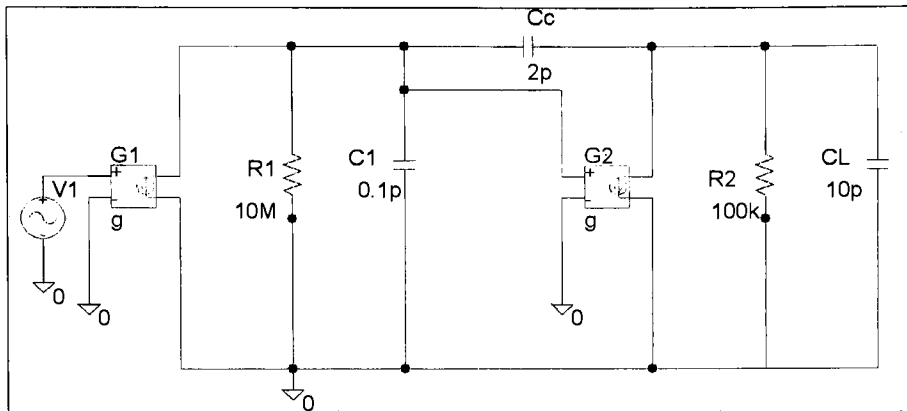


Figure 3.6 Small signal model of a two-stage op-amp

The typical small signal model of the two-stage amplifier is shown in figure 3.6. The resistance $R1$ and capacitance $C1$ are the effective resistance and capacitance seen at the output of the differential stage respectively. The resistance $R2$ and capacitance $C2$ are the effective resistance and capacitance seen at the output of the second stage respectively. The transconductance $G1$, resistance $R1$, and capacitance $C1$ make up the differential stage of the amplifier. The transconductance $G2$, resistance $R2$ and capacitance $C2$ form the output stage of the amplifier. The typical values of the output resistors and the capacitors of the input and the output stage are shown in the figure 3.6 [2].

Here we assume that the internal parasitic $C1$ is much smaller than either the compensation capacitor Cc or the load capacitor $C2$. We can observe from

the equation given below that the location of the right half-plane zero is relative to the unity-gain frequency, which is dependent on the ratio of the transconductance of the two stages. The C_c is parallel to C_1 thereby reducing the pole frequency p_1 by a significant amount. Also, it increases the second pole frequency p_2 via the shunt feedback.

The transfer function of the above small signal model is given as,

$$\text{Transfer Function: } \frac{v_o}{v_i} = \frac{(-s + z)}{(s + w_{p1})(s + w_{p2})} \quad (\text{i})$$

The dominant pole and the second pole is,

$$\text{Dominant pole: } w_{p1} = \frac{1}{R_z g_{mo} R_o C_c} \quad (\text{ii})$$

$$\text{Second pole: } w_{p2} = \frac{g_{mo}}{C_L} \quad (\text{iii})$$

The right half plane zero is located at,

$$\text{RHP zero: } w_z = \frac{g_{mo}}{C_c} \quad (\text{iv})$$

where $g_{mo}=g_{m6}$, $R_z= r_{o2}/r_{o4}$, $R_o=r_{o6}/r_{o7}$, C_c is the compensation capacitor and C_L is the load capacitance.

3.5 Chip package Co-design

Normally the compensation capacitor, which is used to move the dominant pole close to the origin and the second pole away from the origin, occupies almost one-third of the chip area. So in order to minimize this die area, one approach considered was to place the capacitor on the package and to study the stability issues of the amplifier. Thus the following sections talk about the consequences of the stability of the amplifier when the capacitor is placed on the package.

3.5.1 Flip chip Interconnects

Flip chip interconnect is used extensively in the industry as it has a high input-output density capability and also because of its good electrical performance [4]. The solder bumps in the flip chip technology is useful in many ways. It forms the electrical connection between the chip and the substrate. It also may be used as a source for heat dissipation from the chip.

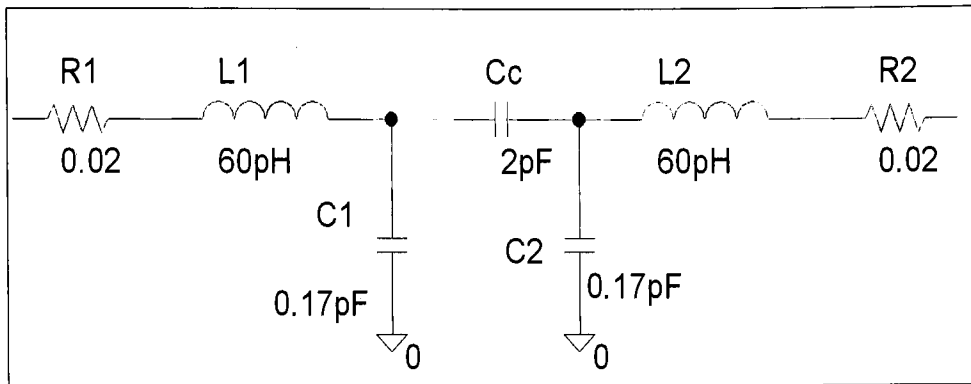


Figure 3.7 Parasitic components due to solder bump interconnects

It may also be used as a structural link between the chip and the substrate. This structural link may affect the electrical and thermal performance of the flip chip interconnects. Degradation in the structural link may be a reliability concern. Figure 3.7 shows the π network formed because of the bump interconnects. The values shown are taken from the packaging research group at Georgia Institute of Technology.

The resistor value for the solder bump is typically 20 m Ω or less. This resistor value is decided by the conductivity of the solder. The inductance value is around 60pH. The capacitor value is typically 0.17pF. The values of the inductor and the capacitor are dominated by the height and diameter of the bump. Also, the underfill material and the pitch may affect the inductance and the capacitance values.

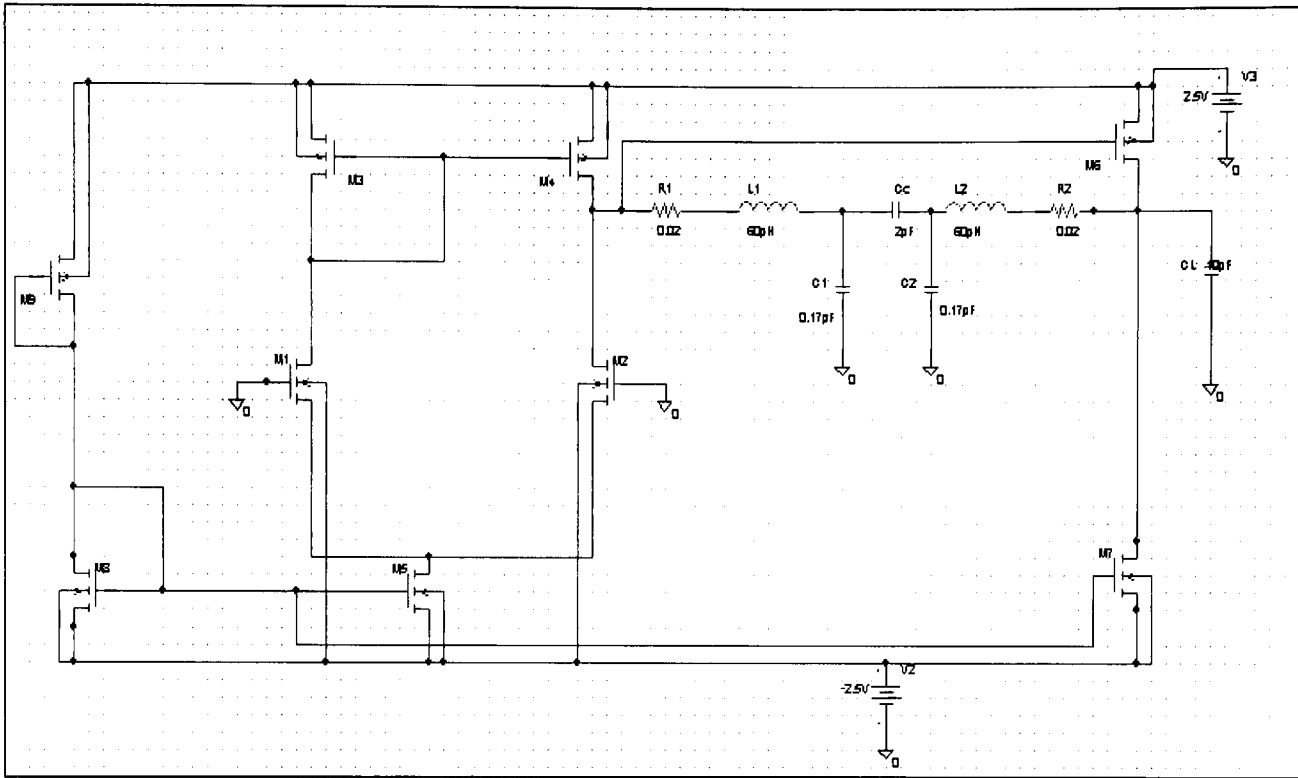


Figure 3.8 Schematic of the op-amp with the parasitic components

Figure 3.8 shows the schematic of the op-amp with the parasitic components formed due to the flip-chip interconnect. In order to find the poles and zeros of the system it is necessary to obtain the transfer function of the small signal model with the parasitic components.

The typical values of the transconductance, output resistance and the output capacitance in the first and the second stage were assumed and the transfer function was calculated.

3.6 Analysis of the small signal model

Applying KCL to each node in figure 3.9 we get the following equations:

$$g_{m1}V_{in} + V_1\left[\frac{1 + sR_{o1}C_{o1}}{(R_{o1})} + \frac{1}{R_1 + sL_1}\right] - \frac{V_2}{R_1 + sL_1} = 0 \quad (3.1)$$

$$-V_1\left[\frac{1}{(R_1 + sL_1)}\right] + V_2\left[\frac{1}{R_1 + sL_1} - sC_1 - sC_c\right] + V_3[sC_c] = 0 \quad (3.2)$$

$$-V_2[sC_c] + V_3[sC_c - sC_2 - \frac{1}{(R_2 + sL_2)}] + V_4\left[\frac{1}{R_2 + sL_2}\right] = 0 \quad (3.3)$$

$$V_4\left[\frac{sR_{o2}C_{o2} + 1}{R_{o2}}\right] + g_{m2} + \frac{1}{R_2 + sL_2} - V_3\left[\frac{1}{R_2 + sL_2}\right] = 0 \quad (3.4)$$

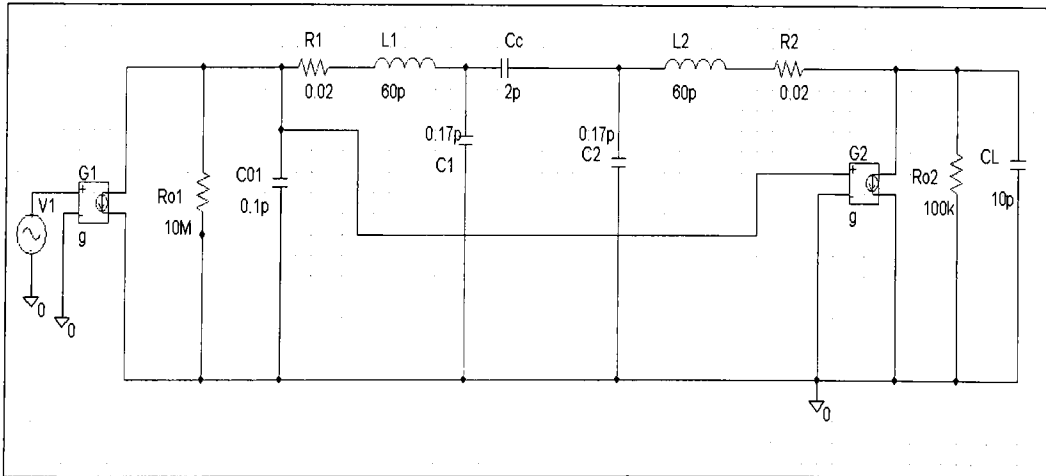


Figure 3.9 Small signal model of the op-amp with parasitic components

Figure 3.9 shows the small signal model of the amplifier with the parasitic. A π network is formed due to the parasitic resistors, capacitors and inductors. The transfer function was derived from the small signal model. Arranging the above equations, the following matrix is obtained.

$$\begin{bmatrix}
 \frac{V_1}{\frac{1+sR_{o1}C_{o1}}{R_{o1}} + \frac{1}{R_1+sL_1}} & \frac{V_2}{\frac{-1}{R_1+sL_1}} & \frac{V_3}{0} & \frac{V_4}{0} \\
 \frac{-1}{R_1+sL_1} & \frac{1}{R_1+sL_1} - sC_1 - sC_c & sC_c & 0 \\
 0 & -sC_c & s(C_c - C_2) \frac{1}{R_2+sL_2} & \frac{1}{R_2+sL_2} \\
 0 & 0 & \frac{-1}{R_2+sL_2} & \frac{sR_{o2}C_{o2}+1}{R_{o2}} + g_{m2} + \frac{1}{R_2+sL_2}
 \end{bmatrix}$$

$$= \begin{bmatrix} -g_{m2}V_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (3.5)$$

To calculate the transfer function, column V_4 is replaced by V_{in} and the following result is obtained,

$$\begin{bmatrix} \frac{1+sR_{o1}C_{o1}}{R_{o1}} + \frac{1}{R_1+sL_1} & \frac{V_2}{R_1+sL_1} & V_3 & V_{in} \\ -1 & \frac{1}{R_1+sL_1} - sC_1 - sC_c & sC_c & 0 \\ 0 & -sC_c & s(C_c - C_2) - \frac{1}{R_2+sL_2} & 0 \\ 0 & 0 & \frac{-1}{R_2+sL_2} & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_{in} \end{bmatrix} = \begin{bmatrix} -g_{m2}V_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$|A|$$

where A is given by the 4x4 matrix in equation 3.5

After solving for V4 we get,

$$\frac{g_{m1}V_{in} \left\{ -\frac{1}{R_1+sL_1} \left[-sC_c \left(\frac{1}{R_2+sL_2} \right) \right] \right\}}{|A|} \quad (3.6)$$

The detailed calculations for the above matrix are shown in Appendix A. After solving this matrix we get a complex transfer function in terms of the parasitic components.

It was found that the transfer function was a huge complex expression with eight poles and two zeros. So, in order to minimize the higher order terms it was necessary to study the impact of each parasitic component on the frequency response of the amplifier. Thus the individual effect of inductance, capacitance and resistance on the frequency response was calculated.

It was found that the resistance did not affect the stability of the amplifier. This is because the poles and the zeros as well as the gain bandwidth frequency were not affected. So the resistance term was eliminated from the transfer function and it was found that the system had a second order zero and a third order pole.

But the third pole and the second order zero were observed at a very high frequency, which was beyond the gain bandwidth frequency. The transfer function was now calculated assuming $R_1=R_2=0$ and assuming that $C_1 = C_2$, $L_1=L_2$.

Hence the simplified transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{(-s^2 + z)}{(s + w_{p1})(s + w_{p2})(s + w_{p3})}$$

The simulations were done and it confirmed the position of the poles and zeros as predicted by the theory.

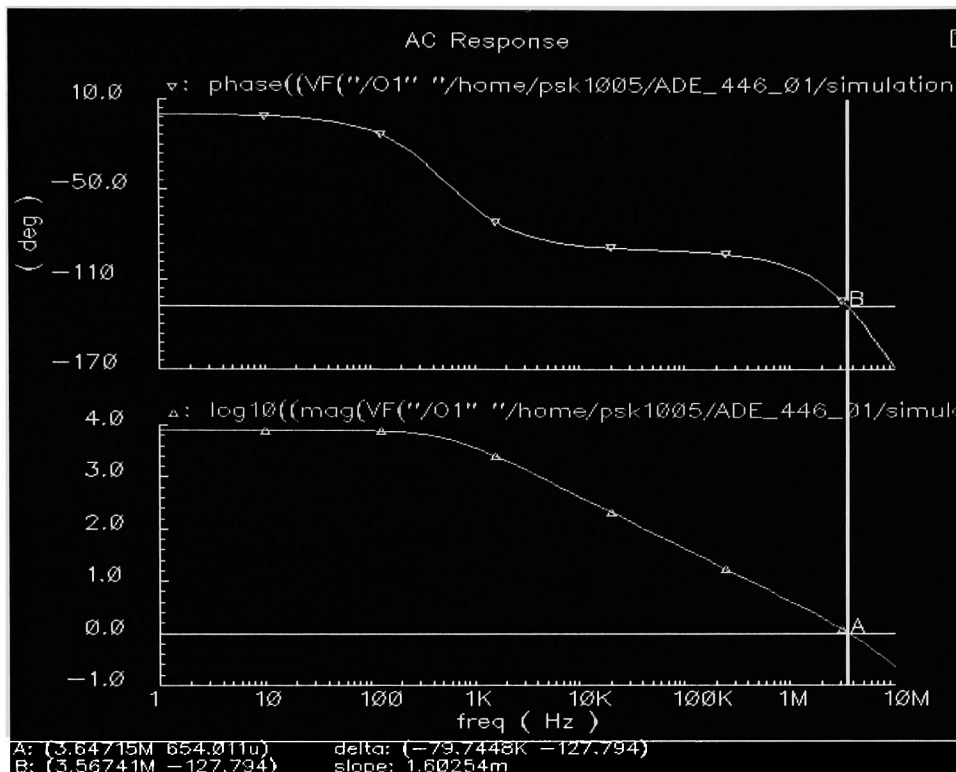


Figure 3.10 Magnitude-Phase plot with parasitic components

Figure 3.10 shows the frequency response when C_c is placed on the package. The gain bandwidth was observed to be 3.64MHz, which is less than the gain bandwidth frequency when C_c was on-chip. Also, the phase margin is considerably large and it was found to be around 52 degrees. From the results shown in table 3.1, it can be observed that the open loop gain of the amplifier is unaffected when the capacitor is placed on the package. The gain bandwidth frequency decreases by a factor of 23%. The phase margin is increased by 2°.

Also the poles of the system are not affected much by placing the capacitor in the package.

Specification	Cc on Chip	Cc on Package
Open loop Gain	2630	2630
Gain Bandwidth Frequency	4.7MHz	3.64MHz
Phase Margin	50.0°	52.3°

**Table 3.1 Comparison of the Specifications with
Cc on the chip and Cc on the Package**

Table 3.1 does a comparison of the specifications when the Cc on the chip and Cc on the package. Thus it can be concluded that placing the capacitor on the package will not affect the stability of the amplifier. As more and more sophisticated packages are made we can make use of these packages by moving the compensation capacitor to the package. For complex systems where the die area is a major issue, we can make use of the concept of chip-package co-design.

Chapter 4

Power supply noise analysis

4.1 Noise

This chapter deals with the effect of power supply noise in the op-amp. In order to improve the performance of op-amps, it is necessary to study its sensitivity to noise. Noise can be categorized as device noise and interference noise. Device noise includes thermal noise, flicker noise and shot noise. Interference noise includes power supply noise and noise due to substrate coupling effect.

4.1.1 Thermal Noise

Thermal noise is generated due to the random motion of electrons in the resistor and it is independent of the current flowing through it. [1]

This noise is proportional to the absolute temperature and resistance and is given by

$$V_n^2 = 4kTRf \quad (4.1)$$

where, k is the Boltzmann constant (1.38×10^{-23} J/K)

T is the absolute temperature

R is the resistance in ohms

f is the bandwidth in hertz

In analog integrated circuits most transistors are operating in saturation region. Noise spectral density in saturation region is expressed as

$$S = 4kT (2/3)g_m \quad (4.2)$$

where g_m is the transconductance. This noise is also called as white noise as the frequency component of this noise source is spread through out the spectrum.

4.1.2 Flicker Noise

Flicker noise is the dominant source of noise in MOSFET devices at low frequencies. Flicker noise basically arises due to the random trapping and detrapping of charges in the oxide traps near the silicon substrate and the gate oxide interface [1]. This noise source is also called as $1/f$ noise as the noise spectral density is inversely proportional to the frequency.

The flicker noise is expressed as

$$V_n^2 = \frac{K}{C_{ox}WL} \frac{1}{f} \quad (4.3)$$

where K depends on the temperature and process. A typical value of K is $3.0 \times 10^{-24} \text{ V}^2$.

4.1.3 Shot Noise

Shot noise is caused by the random fluctuations in the motion of the charge carriers in a conductor [4]. Thus it is dependent on the flowing current.

The shot noise is given by

$$I = \sqrt{2qI_{bias}\Delta f} \quad (4.4)$$

where I is the rms shot noise and q is the charge of an electron. In a conducting MOSFET normally the charge density is high and the electric field is low. Thus equation (4.4) does not hold for MOSFET's.

4.2 Noise in Operational Amplifiers

Noise can be any random signal, which is found at the output of the amplifier that cannot be predicted by the AC or DC input analysis. The main sources of noise in CMOS op-amps are the $1/f$ noise and the thermal noise [1]. The flicker noise is the dominant source of noise at low frequencies and the thermal noise is dominant at high frequencies.

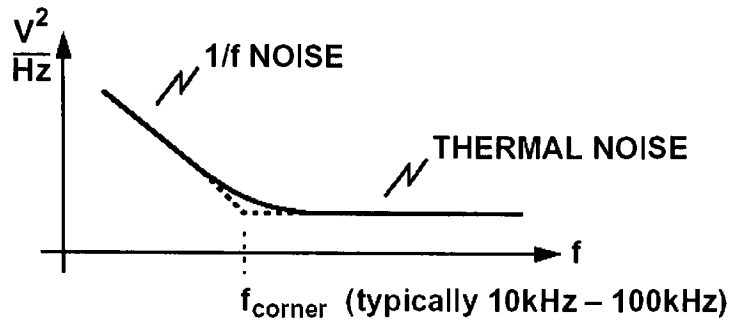


Figure 4.1[9] Noise vs. Frequency graph

Noise in the op-amp is specified with the help of the graph between input-referred noise and the frequency as shown in figure 4.1. The corner frequency is the frequency in the spectrum where the $1/f$ noise and the thermal noise are equal. The noise of the overall op-amp is dominated by the noise contributions from the input stage transistors. The reason is that the input noise is magnified by the gain provided by the differential stage and the high gain output stage.

The noise at the input, if present, is multiplied by the gain of the amplifier along with the original input signal. Therefore, it is important to predict the causes of noise and devise measures to eliminate it. Figure 4.3 shows the differential pair with the noise generated by each transistor represented by a voltage source.

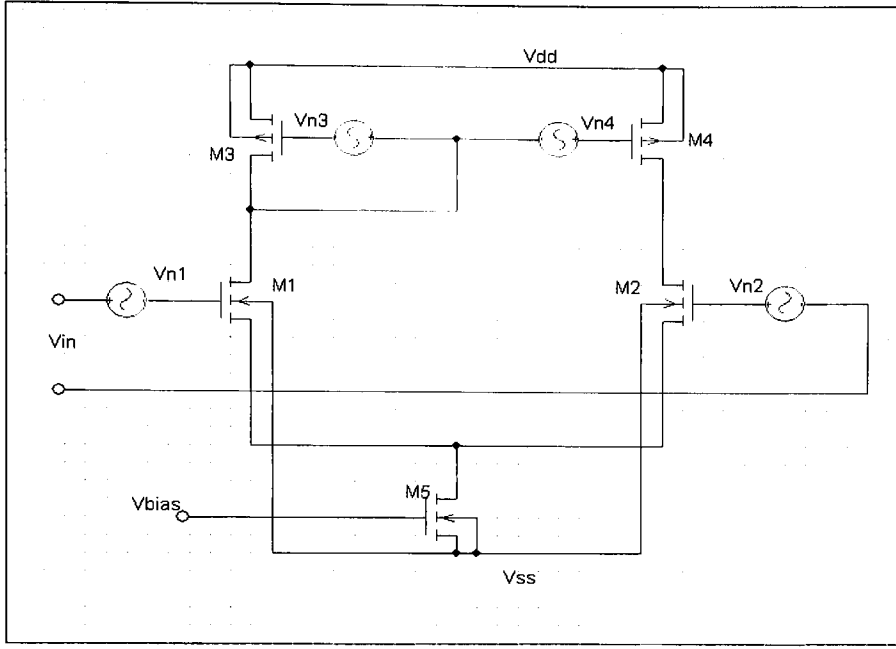


Figure 4.2 Noise sources in the Differential Amplifier

To calculate the flicker noise and the thermal noise, we model the noise as voltage sources in series with the gates of the transistors [1]. The voltage gain provided by the differential stage to the input noise sources is given by

$$A_d = g_{m1}(r_{o2} // r_{o4}) \quad (4.5)$$

Similarly the gain for the noise sources on the gates of the active load transistors can be calculated. The noise source v_{n3} introduces a noise current in transistor M3 which is mirrored in transistor M4.

Thus, the overall gain at the output stage of the single ended differential amplifier is given by,

$$V_{\text{input}}^2 = v_{n1}^2 + v_{n2}^2 + \left(\frac{g_{m4}}{g_{m1}} \right)^2 (v_{n3}^2 + v_{n4}^2) \quad (4.6)$$

Thus to minimize the noise at the input it can be seen from equation 4.6 that the transconductance of transistor M1 should be larger than the transconductance of M4. The input transistors M1 and M2 are the dominant sources of noise.

4.3 Power supply Noise

Many difficulties are encountered due to the parasitics being associated with the package. The difficulties are experienced at high speeds of the circuits, where the actual performance is difficult to evaluate. Some of the parasitics include: bond wire self-inductance, trace-to-trace capacitance, trace-to-ground capacitance, trace-to-trace mutual inductance, and trace self-inductance [1]. During each clock transition, significant noise is generated on the supply and the ground planes due to the fact that switching occurs between digital gates on a large scale [13]. It is not always practical to have separate supply lines for digital and analog circuits. It would be prudent to acknowledge that the noise on

the power supply can significantly affect the sensitivity of the amplifier. This is due to the fact that coupling occurs between various parts on the package.

As the frequency of operation of the digital systems increases, the interconnection between the circuit elements causes a number of problems. When a rapid change of voltage occurs at one end of the supply line because of switching, this transient travels along the line to the far end [14]. Power supply may be a reason for generating internal noise. Because of the operation of the logic circuits, a large current transient may be produced in the power supply lines, which in turn develops a voltage across them [8]. The ground line cannot be considered at a voltage equivalent to zero volts.

The noise may be either internally generated because of the switching of the circuits or it may be produced by external sources like pick-up of electromagnetic radiation. This power supply noise can occur in any part of the system like on-chip or in the package [9]. Hence, it is an important task to understand this source of noise and to study the effects of this noise on the performance of the system.

4.4 Analysis of Power supply noise in op-amp

Noise is the fundamental limitation on the performance of the op-amp. It is important to know how the power supply noise affects the op-amp specifications and the overall performance of the operational amplifier. As shown in the schematic the noise is injected via the supply voltage, which is connected to the source contact of the PMOS transistors. It is required to calculate the noise voltage at the output due to variations on the power supply.

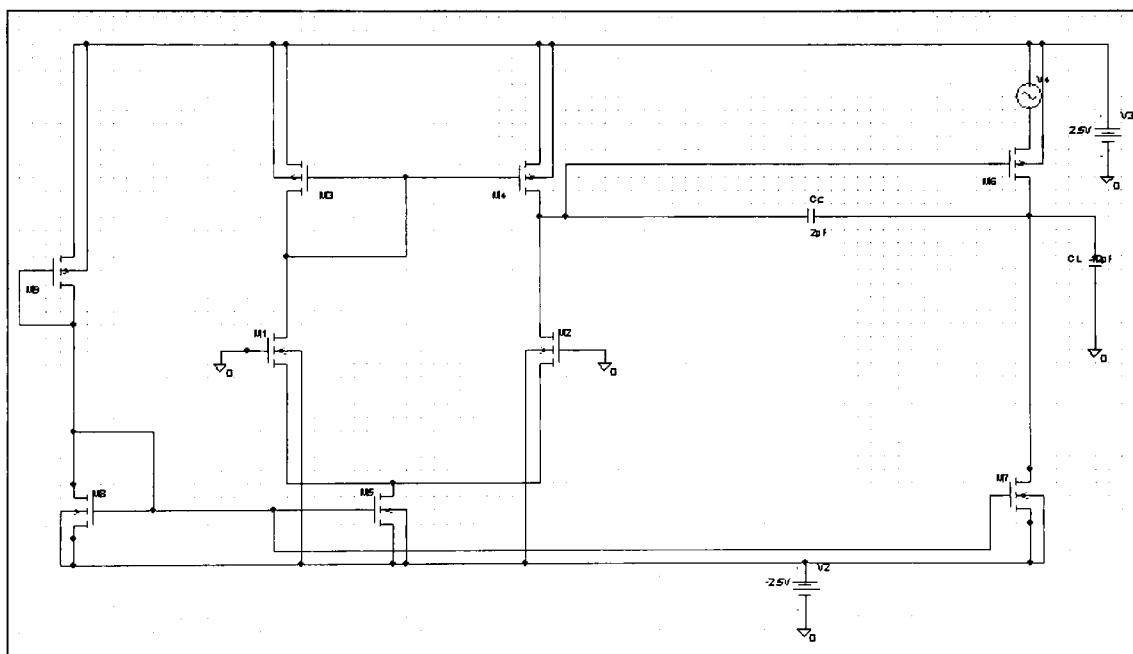


Figure 4.3 Power Supply noise in the CMOS op-amp

The power supply noise can be coupled to the output through three different circuit paths. The individual contribution to the output noise voltage by each of the paths is determined and then the total effect is studied. The first path

considered is the noise coupled to the output through the transistor M6. The noise is injected at the source terminal of transistor M6 as shown in figure 4.3. When noise is injected at the source of the transistor M6, it can be considered as a common gate configuration.

In order to obtain the output noise voltage we apply the Kirchoff's voltage law and derive the following equation,

$$g_{m6}V_{GS6} + \left(\frac{-V_{out} + V_{GS6}}{r_{o6}} \right) = \frac{V_{out}}{r_{o7}} \quad (4.7)$$

where g_{m6} is the transconductance of transistor M6 and r_{o6} , r_{o7} are the equivalent output resistances of transistors M6 and M7 respectively.

The DC gain can be expressed as

$$A_{oL} = g_{m6}(r_{o6} // r_{o7}) \quad (4.8)$$

Therefore the transfer function is

$$\frac{V_{out}}{V_{in6}} = \frac{g_{m6}(r_{o6} // r_{o7})}{1 + \frac{j\omega}{fp1}} \quad (4.9)$$

$$\text{where } fp1 = \frac{1}{2\pi((r_{o6} // r_{o7}))C_L} \quad (4.10)$$

where C_L is the load capacitor. Substituting the values of the transconductance g_{m6} and the output resistance $r_{o6}||r_{o7}$, we get the corresponding gain values for different input frequencies.

Frequency (Hz)	Gain
1k	11.2026
10k	10.91
50k	7.64
100k	4.72
200k	2.43
500k	0.77

Table 4.1 Frequency vs. Gain for M6 transistor

The variation of gain with frequency for transistor M6 is plotted in figure 4.4. The transconductance and the output resistance values were calculated. These values were used to calculate the theoretical gain. The table 4.1 shows the gain of the power supply noise at the output stage for the corresponding frequency values. Thus, it was observed that output stage of the amplifier showed a flat response upto 1kHz. It was found that in this case there was only one pole generated due to the load capacitor.

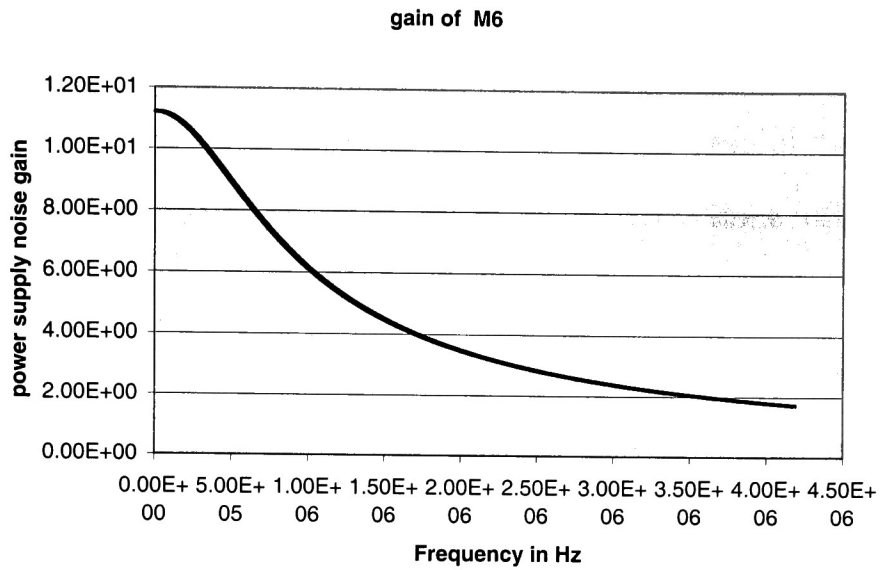


Figure 4.4 PS noise gain vs. Frequency plot for M6 transistor

(Theoretically calculated)

Figure 4.5 shows the simulation results for the gain versus frequency plot.

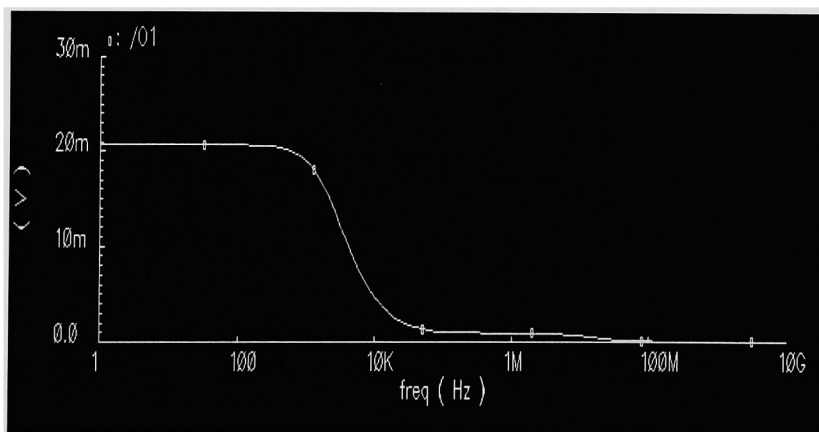


Figure 4.5 PS noise gain vs. frequency plot (Simulation results)

From figures 4.4 and 4.5 it can be seen that the theoretical and the simulation results agree well. The gain was found to be equal to 20 at low frequencies and rolls down as frequency increases. In case of the theoretical result, the gain was found to be 11 for low frequencies and starts rolling off as the frequency increases.

The second circuit path for noise coupling is through transistor M4. The gain when the input is applied to the source of M4 was calculated. Figure 4.6 shows the small signal model of the circuit when the power supply noise is applied to the transistor M4.

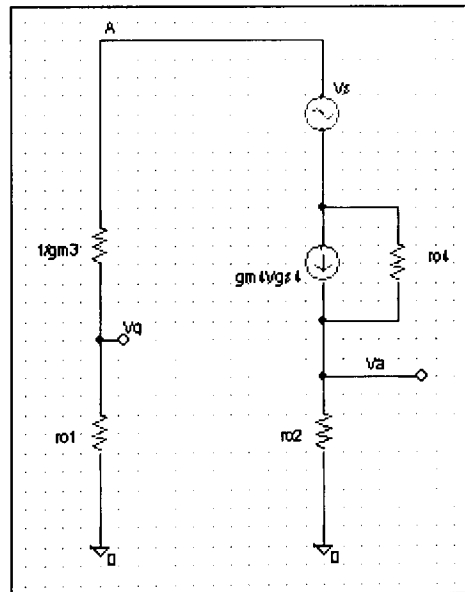


Figure 4.6 Small signal model for the differential pair

Let I_3 be the current that flows through the branch “A” as indicated in figure 4.6.

The effective resistance of this branch is the series combination of r_{o1} and $\frac{1}{g_{m3}}$.

Nodal analysis on the small signal model yields the following equations.

$$I_3 = \frac{-V_G}{r_{o1}} = \frac{V_G - V_s}{\frac{1}{g_{m3}}} \quad (4.11)$$

$$g_{m3}(V_G - V_s) = \frac{-V_G}{r_{o1}}$$

Calculating V_G in terms of V_s ,

$$V_G = \frac{V_s}{1 + \frac{1}{g_{m3}r_{o1}}} \quad (4.12)$$

$$I_3 = g_{m4}V_{GS4} + I_4 = \frac{V_{out}}{r_{o2}} \quad (4.13)$$

where, r_{o1} and r_{o2} are the equivalent output resistances of transistor M1 and M2 respectively and g_{m3} and g_{m4} are the transconductances of transistor M3 and M4 respectively.

Thus, rearranging the equations and calculating V_A in terms of the output voltage we get,

$$\frac{V_{out}}{V_{in4}} = \frac{\frac{\frac{g_{m4}}{1} - g_{m4} + \frac{1}{r_{o4}}}{1 + \frac{1}{r_{o1}g_{m3}}}}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}}} \quad (4.14)$$

The overall gain seen at the output of the op-amp is given as

$$\frac{V_{out}}{V_{in4}} = \frac{\frac{[\frac{g_{m4}}{1}] - g_{m4} + \frac{1}{r_{o4}}}{1 + \frac{1}{r_{o1}g_{m3}}} - g_{m6}(r_{o6} // r_{o7})}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}}} \times \frac{1}{\sqrt{1 + \frac{f^2}{f_{p1}^2}} \sqrt{1 + \frac{f^2}{f_{p2}^2}}} \quad (4.15)$$

$$\text{where } f_{p1} = \frac{1}{2\pi(r_{o4} // r_{o2})C_c[1 + g_{m6}(r_{o6} // r_{o7})]}$$

$$\text{and } f_{p2} = \frac{1}{2\pi(r_{o6} // r_{o7})[C_l + C_c[1 + \frac{1}{g_{m6}(r_{o6} // r_{o7})}]]}$$

The third path for noise coupling is through transistor M3. But this path is neglected because, the diode-connected configuration of M3 does not contribute much to the overall gain of the op-amp. Hence the amplification of noise is also negligible. Thus, the transistors that will contribute to the amplification of noise

voltage in the op-amp are transistors M4 and M6. The noise seen at the output is the summation of the overall noise calculated at each node of these transistors.

Table 4.2 shows the variation of differential gain with frequency for transistor M4. The overall gain seen at the output of the op-amp is the product of this differential gain and the output stage gain.

Frequency (Hz)	Gain
1k	61.27
10k	59.69
50k	41.81
100k	25.87
200k	13.33
500k	4.26
800k	2.03
1M	1.38

Table 4.2 Gain vs. frequency for M4 Transistor

As the frequency increases the gain starts rolling down. The transistor M4 contributes most to the effective output noise voltage. So it is important to study the effect of the power supply noise particularly in this bandwidth region. Also, the compensation capacitor adds an additional pole to the system resulting in a two- pole system.

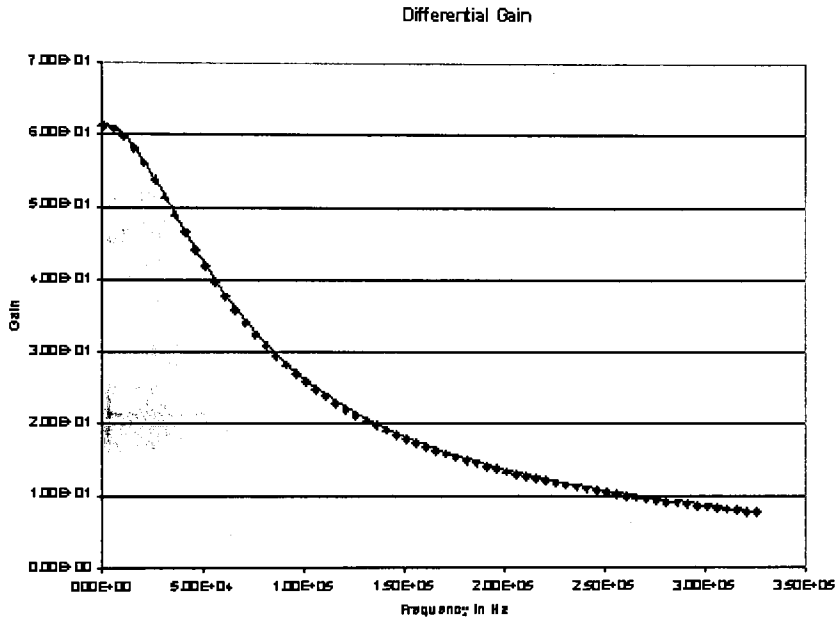


Figure 4.7 Gain vs. Frequency plot for transistor M4
(Theoretically calculated)

The differential gain was calculated using equation 4.14. The output stage is in the common source configuration.

Thus, the output stage gain is given as

$$\frac{V_{out}}{V_6} = -g_{m6}(r_{o6} // r_{o7}) \quad (4.16)$$

This output stage gain is multiplied by the differential gain, which gives the overall gain and is given by the following equation,

$$\frac{V_{out}}{V_{in4}} = \frac{\frac{\frac{g_{m4}}{1 + \frac{1}{r_{o1}g_{m3}}} - g_{m4} + \frac{1}{r_{o4}}}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}}} x - g_{m6}(r_{o6} // r_{o7})}{\sqrt{1 + \frac{f^2}{f_1^2}} \sqrt{1 + \frac{f^2}{f_2^2}}} \quad (4.17)$$

Table 4.3 shows the variation of power supply noise gain with frequency.

Frequency (Hz)	Gain
1k	686.49
10k	668.67
50k	466.99
100k	274.42
200k	142.77
500k	37.86

Table 4.3 Frequency vs. gain for the M4 transistor and the output stage

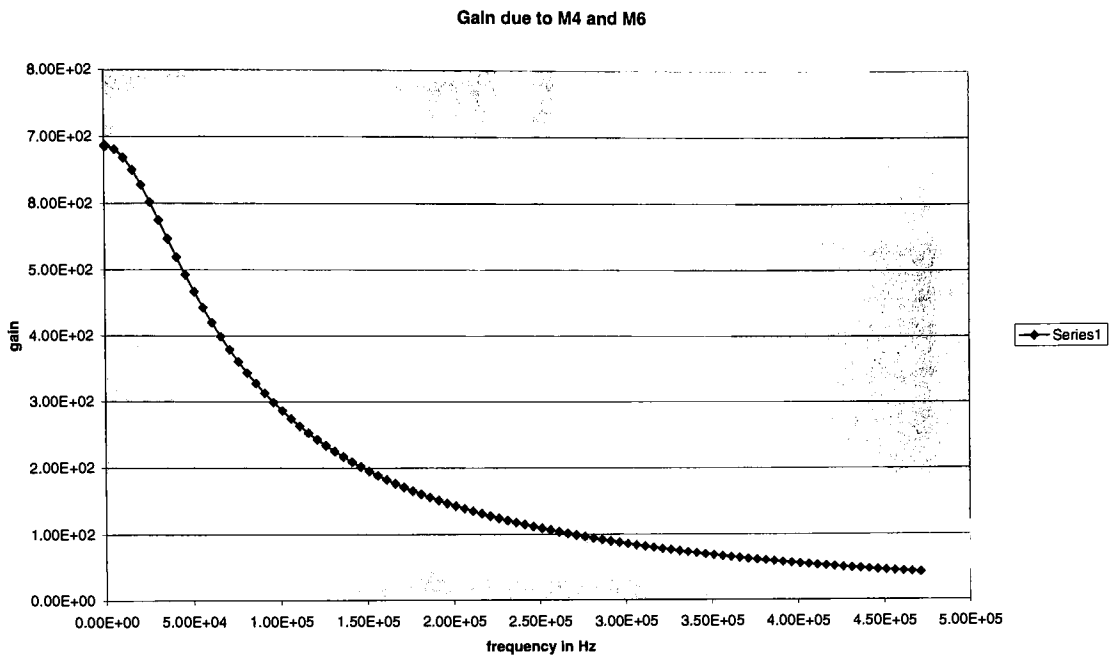


Figure 4.8 Gain vs. Frequency graph for transistor M4 and the output stage
(Theoretically calculated)

Figure 4.8 shows the plot of gain versus frequency as calculated using equation 4.17. The simulation results shows that the gain starts out at 1050 for low frequencies and remains constant till about 2kHz and then starts rolling off as the frequency continues to increase. Figure 4.9 shows the plot of simulated result for the overall power supply noise gain vs. the frequency for transistor M4.

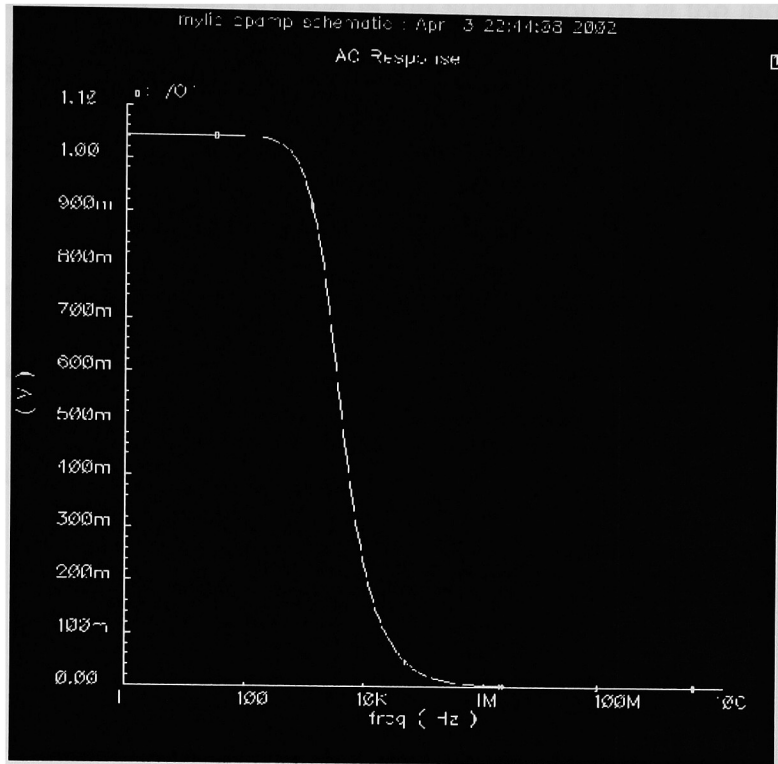


Figure 4.9 Gain vs. Frequency for transistor M4

(Simulated Results)

It was found that the theoretical and simulated results agree well. The paths that provide maximum contribution to the amplification of the noise voltage in the power supply have been analyzed. From the analysis and the results it is evident that the noise in the power supply affects the performance of the system considerably. It is therefore necessary to account for this noise.

The total output noise voltage is the summation of all the individual output noise generated by the three different circuit paths. The input referred noise is the output noise voltage divided by the gain. This noise indicates how much the input signal is corrupted by the noise in the circuit. The input referred noise is a conceptual phenomenon. In practice it is not possible to measure the noise present at the input of the circuit.

Thus the input referred noise is given by,

$$V_{in}^2 = \frac{V_{out}^2}{A_v^2} \quad (4.18)$$

where V_{out}^2 is the output noise voltage and A_v^2 is the gain of the system.

In case of the op-amp the total output noise voltage was measured to be 1.07V. As seen earlier the gain of the amplifier was observed to be 2630. Thus the input noise is 0.406mV. The signal-to-noise ratio (SNR) is

$$SNR = 20 \log (V_{in}/V_{nv}) \quad (4.19)$$

Where, V_{nv} is the input referred noise. In a system assume that the desired input signal to noise ratio is 60dB and the input signal has an amplitude of 10mV. Then, the maximum allowable input referred noise will be 1 μ V. Knowing that the gain of the op-amp is 2630, the maximum output noise voltage can be calculated and it was found to be 2.63mV. In the case of the op-amp discussed earlier the output noise voltage was too high. This high output noise voltage may affect the

output signal, which will in turn, affect the performance of the op-amp. Similar analysis can be done for the output signal-to-noise ratio. Thus in order to overcome this problem, one solution is to increase the level of the input signal. This input signal may depend on the application of the system. Therefore it is not always feasible to increase this input signal. Another solution is to study the placement of the op-amp on the package, so that the magnitude of the noise voltage on the power supply is lesser.

Chapter 5

Conclusion

The chip-package co-design of a low voltage CMOS two-stage operational amplifier was presented in this thesis. The main purpose of chip-package co-design is to study the effect of moving the passive components to the package. The advantage of doing so is to reduce the chip area and also it has been found that the passives in the package have better quality factor. By saving the chip area, more number of functional blocks can be accommodated on-chip. The development of sophisticated packages makes it feasible to enhance the chip-package co-design concept. It is a novel concept and no prior work has dealt with this type of analysis.

The stability issues when C_c is placed on the package were considered in the thesis. The compensation capacitor is used to shift the dominant pole closer to the origin and the second pole away from the origin. When this capacitor is placed on the package, due to the solder bumps, parasitics are formed at both nodes of the capacitor. The effect of these parasitics on the op-amp specifications was studied. A comparison was made between the C_c on the chip and the C_c on the package. From the results it was observed that the stability of the op-amp was not affected much when the C_c was placed in the package.

Table 5.1 shows the comparison between C_c on-chip and C_c on package.

Specification	Cc on Chip	Cc on Package
Open loop Gain	2800	2800
Gain Bandwidth Frequency	4.7MHz	3.64MHz
Phase Margin	50.0°	52.3°

Table 5.1 Results of Cc on chip and Cc on package

It can be seen from the table that the gain bandwidth of the op-amp decreases when the Cc is on the package but is within tolerable limits. The phase margin increases by 2 degrees. Thus, it can be concluded that for an op-amp design it does not make a significant difference as to whether the capacitor is placed on-chip or in the package.

The position of the poles and the zeros of the system were determined theoretically and were compared with the simulation results. It was observed from the transfer function of the op-amp that the system had three poles and 2 zeros. Appendix A shows the theoretical calculations for the transfer function of the op-amp with the parasitics introduced by the flip-chip interconnects. The third pole and the second order zero were observed at a very high frequency, which was much beyond the gain bandwidth frequency of the op-amp.

The second part of the thesis discusses the effect of power supply noise on the op-amp. The same two-stage low voltage op-amp was used for analysis. A theoretical analysis to determine the output noise voltage due to noise on the power supply was done. Typical noise sources like thermal and flicker noise that affect the performance of the op-amp is also discussed. The source of the power supply noise is explained in the thesis.

Typically in high-speed systems it is very critical to design the power planes. During each clock transition significant noise is generated on the supply and the ground planes due to the fact that switching occurs between digital gates on a large scale. It is important to study the impact of this power supply noise on the system.

The noise source in the power supply was represented as a voltage source and was injected in each node of the transistor, which is connected to the power supply. Theoretically, the gain provided by the op-amp to the noise voltage was calculated. The noise at each node was then added together to get the overall noise at the output stage.

The experimental results and the theoretical values matched well. The simulated results showed that the overall gain of the op-amp was 1050 and the theoretical results showed an overall gain of 686. Thus, it is observed that the power supply noise contributes significantly to the noise at the output of the

amplifier. Therefore, proper care must be taken in the design in order to reduce this noise.

Future Work

The immediate focus would be to fabricate a test chip and take measurements. The layout for the designed op-amp was done using Virtuoso Layout Editor. The chip area was found to be $100\mu\text{m} \times 69.71\mu\text{m}$ out of which the compensation capacitor occupied $66.41\mu\text{m} \times 69.71\mu\text{m}$.

Knowing the impedance profile of the chip along with the information about the noise voltage variation on the power supply, a placement methodology can be developed for the op-amp in order to enhance the performance.

It would also be interesting to study the effect of shrinking the power supply voltage on the sensitivity of op-amp. Applications where op-amps are used can be used to study the power supply noise effects pertaining to their respective specifications.

References

- [1] Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill Inc., 2001.
- [2] Phillip E.Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Holt, Rinehart, and Winston, Inc., New York 1987.
- [3] Jiri Dostal, "Operational Amplifiers", Butterworth-HeinemannInc., 1993.
- [4] Paul R.Gray and Robert G. Meyer, " Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, Inc., 1984.
- [5] Bhupendra K.Ahuja, " An Improved Frequency Compensation Technique for CMOS Operational Amplifier", *IEEE Journal of Solid-State Circuits*, Vol.SC-18, No.6, pp.629-633, Dec.1983.
- [6] G. Giustolisi, G.Palmisano, G.Palumbo, and T.Segreto, "1.2V CMOS Op-Amp with a Dynamically Biased Output Stage", *IEEE Journal of Solid-State Circuits*, Vol. 35, No.4, pp.632-636, April 2000.
- [7] Jerald G.Graeme, "Applications of Operational Amplifiers", McGraw-Hill Inc., 1973.
- [8] C.W. Fok and D.L. Pulfrey, "Full-Chip Power Supply Noise: The effect of on-chip power-rail Inductance" , *International Journal of High Speed Electronics and Systems*, pp 1-10.
- [9] W.S. Song and L.A. Glasser, " Power Distribution techniques for VLSI Circuits", *IEEE Journal for Solid-State Circuits*, SC-9, pp 150-156, 1986.

- [10] Satoshi Sakurai and Mohammed Ismail, " Low-Voltage CMOS Operational Amplifiers" , Kluwer Academic Publishers, 1995.
- [11] Kevin M. Daugherty, " Analog-to-Digital Conversion", McGraw-Hill Inc.,1995.
- [12] K.Bult and A.Buchwald, "An embedded 240-mW 10-b 50- MS/s CMOS ADC in 1-mm² ", *IEEE J.o7 Solid-State Circuits*, vol 32, no.12, pp.1887-1895, Dec. 1990.
- [13] H.Parthasarathy, G.Nayak and P.R.Mukund, " Analysis of VCO Jitter
- [14] N.K.Verghese, T.J.Schmerbeck, and D.J.Allstot, "Simulation Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits", Boston:Kluwer Academic Publishers,1995.
- [15] R. Gregorian, " Introduction to CMOS op-amps and Comparators", John Willey & sons,Inc., 1999.

Appendix A

Calculations for the transfer Function

$$g_{m1}V_{in} + V_1\left[\frac{1 + sR_{o1}C_{o1}}{(R_{o1})} + \frac{1}{sL_1}\right] - \frac{V_2}{sL_1} = 0 \text{-----(A.1)}$$

$$-V_1\left[\frac{1}{(sL_1)}\right] + V_2\left[\frac{1}{sL_1} - sC_1 - sC_c\right] + V_3[sC_c] = 0 \text{-----(A.2)}$$

$$-V_2[sC_c] + V_3[sC_c - sC_2 - \frac{1}{(sL_2)}] + V_4\left[\frac{1}{sL_2}\right] = 0 \text{-----(A.3)}$$

$$V_4\left[\frac{sR_{o2}C_{o2} + 1}{R_{o2}} + g_{m2} + \frac{1}{sL_2}\right] - V_3\left[\frac{1}{sL_2}\right] = 0 \text{-----(A.4)}$$

$$\begin{bmatrix} \frac{1+sR_{o1}C_{o1}}{R_{o1}} + \frac{1}{sL_1} & \frac{V_2}{sL_1} & V_3 & V_{in} \\ \frac{-1}{sL_1} & \frac{1}{sL_1} - sC_1 - sC_c & sC_c & -g_{m1}V_{in} \\ 0 & -sC_c & s(C_c - C_2) - \frac{1}{sL_2} & 0 \\ 0 & 0 & \frac{-1}{sL_2} & 0 \end{bmatrix}$$

A

$$\frac{1+sR_{o1}C_{o1}}{R_{o1}} + \frac{1}{sL_1} \begin{bmatrix} \frac{1}{sL_1} - sC_1 - sC_c & sC_c & 0 \\ -sC_c & sC_c - sC_1 - \frac{1}{sL_1} & 0 \\ 0 & -\frac{1}{sL_1} & 0 \end{bmatrix}$$

$$+ \frac{1}{sL_1} \begin{bmatrix} -\frac{1}{sL_1} & sC_c & 0 \\ 0 & sC_c - sC_1 - \frac{1}{sL_1} & 0 \\ 0 & -\frac{1}{sL_1} & 0 \end{bmatrix}$$

$$+ g_{m1} V_{in} \begin{bmatrix} \frac{-1}{sL_1} & \frac{1}{sL_1} - sC_1 - sC_c & sC_c \\ 0 & -sC_c & sC_c - sC_1 - \frac{1}{sL_1} \\ 0 & 0 & \frac{-1}{sL_1} \end{bmatrix}$$

$$+ \begin{bmatrix} -\frac{1}{sL_1} & sC_c & 0 \\ 0 & sC_c - sC_1 - \frac{1}{sL_1} & 0 \\ 0 & -\frac{1}{sL_1} & 0 \end{bmatrix}$$

$$\therefore g_{m1} V_{in} \left[\frac{-1}{sL_1} \left(\frac{C_c}{L_1} \right) - \left[\frac{1}{sL_1} - sC_1 - sC_c \right] 0 + sC_c (0) \right]$$

$$\therefore -g_{m1} V_{in} \left[\left(\frac{C_c}{sL_1^2} \right) \right] = \text{Numerator}$$

For solving the determinant A

$$\frac{1 + sR_{o1}C_{o1}}{R_{o1}} + \frac{1}{sL_1} \begin{bmatrix} \frac{1}{sL_1} - sC_1 - sC_c & sC_c & 0 \\ -sC_c & sC_c - sC_1 - \frac{1}{sL_1} & \frac{1}{sL_1} \\ 0 & -\frac{1}{sL_1} & g_{m2} + \frac{1 + sR_{o2}C_{o2}}{R_{o2}} + \frac{1}{sL_1} \end{bmatrix}$$

$$+ \frac{1}{sL_1} \begin{bmatrix} -\frac{1}{sL_1} & sC_c & 0 \\ 0 & sC_c - sC_1 - \frac{1}{sL_1} & \frac{1}{sL_1} \\ 0 & -\frac{1}{sL_1} & g_{m2} + \frac{1 + sR_{o2}C_{o2}}{R_{o2}} + \frac{1}{sL_1} \end{bmatrix}$$

$$\therefore \left(\frac{1 + sR_{o1}C_{o1}}{R_{o1}} + \frac{1}{sL_1} \right) \times \left[\left(\frac{1}{sL_1} - sC_1 - sC_c \right) \left\{ \left(sC_c - sC_1 - \frac{1}{sL_1} \right) \left(g_{m2} + \frac{1 + sR_{o2}C_{o2}}{R_{o2}} + \frac{1}{sL_1} \right) + \frac{1}{s^2 L_1^2} \right\} \right. \\ \left. + sC_c \left\{ sC_c \right\} \left(g_{m2} + \frac{1 + sR_{o2}C_{o2}}{R_{o2}} + \frac{1}{sL_1} \right) \right] \\ \frac{1}{sL_1} \left[\left(\frac{-1}{sL_1} \right) \left\{ sC_c g_{m2} + \frac{sC_c + s^2 R_{o2} C_{o2}}{R_{o2}} + \frac{C_c}{L_1} - s g_{m2} C_1 - \frac{sC_1 - s^2 R_{o2} C_{o2} C_1}{R_{o2}} - \frac{C_1}{L_1} \right\} \right. \\ \left. - \frac{g_{m2}}{sL_1} - \frac{(1 + sR_{o2}C_{o2})}{sL_1 R_{o2}} - \frac{1}{s^2 L_1^2} + \frac{1}{s^2 L_1^2} \right]$$

$$\begin{aligned}
& \therefore \left(\frac{1 + sR_{o1}C_{o1}}{R_{o1}} + \frac{1}{sL_1} \right) \\
& \left[\left(\frac{1}{sL_1} - sC_1 - sC_c \right) \left(sg_{m2}C_c + \left(\frac{sC_c + s^2R_{o2}C_{o2}C_c}{R_{o2}} \right) + \frac{C_c}{L_1} - sg_{m2}C_1 - \frac{sC_1 - s^2R_{o2}C_{o2}C_1}{R_{o2}} \right) \right. \\
& \quad \left. - \frac{C_1}{L_1} - \frac{g_{m2}}{sL_1} - \left(\frac{1 + sR_{o2}C_{o2}}{sL_1R_{o2}} \right) - \cancel{\frac{1}{s^2L_1^2}} + \cancel{\frac{1}{s^2L_1^2}} \right) \\
& \quad \left. + sC_c \left(sC_c g_{m2} + \frac{sC_c + s^2R_{o2}C_{o2}C_c}{R_{o2}} + \frac{C_c}{L_1} \right) \right] \\
& + \frac{1}{sL_1} \left[\left(\frac{-1}{sL_1} \right) \left\{ sC_c g_{m2} + \frac{sC_c + s^2R_{o2}C_{o2}}{R_{o2}} + \frac{C_c}{L_1} - sg_{m2}C_1 - \frac{sC_1 - s^2R_{o2}C_{o2}C_1}{R_{o2}} - \frac{C_1}{L_1} \right\} \right. \\
& \quad \left. - \frac{g_{m2}}{sL_1} - \frac{(1 + sR_{o2}C_{o2})}{sL_1R_{o2}} - \cancel{\frac{1}{s^2L_1^2}} + \cancel{\frac{1}{s^2L_1^2}} \right]
\end{aligned}$$

$$\begin{aligned}
& \therefore \left(\frac{1 + sR_{o1}C_{o1}}{R_{o1}} + \frac{1}{sL_1} \right) \\
& \left[\left(\frac{1}{sL_1} - sC_1 - sC_c \right) \left(sg_{m2}C_c + \left(\frac{sC_c + s^2R_{o2}C_{o2}C_c}{R_{o2}} \right) + \frac{C_c}{L_1} - sg_{m2}C_1 - \frac{sC_1 - s^2R_{o2}C_{o2}C_1}{R_{o2}} \right) \right. \\
& \quad \left. - \frac{C_1}{L_1} - \frac{g_{m2}}{sL_1} - \left(\frac{1 + sR_{o2}C_{o2}}{sL_1R_{o2}} \right) \right) \\
& \quad \left. + sC_c \left(sC_c g_{m2} + \frac{sC_c + s^2R_{o2}C_{o2}C_c}{R_{o2}} + \frac{C_c}{L_1} \right) \right] \\
& + \frac{1}{sL_1} \left[\left(\frac{-1}{sL_1} \right) \left\{ sC_c g_{m2} + \frac{sC_c + s^2R_{o2}C_{o2}}{R_{o2}} + \frac{C_c}{L_1} - sg_{m2}C_1 - \frac{sC_1 - s^2R_{o2}C_{o2}C_1}{R_{o2}} - \frac{C_1}{L_1} \right\} \right. \\
& \quad \left. - \frac{g_{m2}}{sL_1} - \frac{(1 + sR_{o2}C_{o2})}{sL_1R_{o2}} \right]
\end{aligned}$$

$$\therefore \left(\frac{1 + sR_{o1}C_{o1}}{R_{o1}} + \frac{1}{sL_1} \right) \left[\begin{aligned} & \frac{g_{m2}C_c}{L_1} + \frac{C_c + sR_{o2}C_{o2}C_c}{L_1R_{o2}} + \frac{C_c}{sL_1^2} - \frac{g_{m2}C_1}{L_1} - \frac{C_1 - sR_{o2}C_{o2}C_1}{R_{o2}L_1} - \frac{C_1}{sL_1^2} - \frac{g_{m2}}{s^2L_1^2} \\ & - \frac{(1 + sR_{o2}C_{o2})}{s^2L_1^2R_{o2}} - s^2g_{m2}C_cC_1 - \frac{s^2C_cC_1 - s^3R_{o2}C_{o2}C_cC_1}{R_{o2}} - \frac{sC_cC_1}{L_1} + s^2g_{m2}C_1^2 \\ & + \frac{s^2C_1^2 + s^3R_{o2}C_{o2}C_1^2}{R_{o2}} + \frac{sC_1^2}{L_1} + \frac{g_{m2}C_1}{L_1} + \frac{(C_1 + sR_{o2}C_{o2}C_1)}{L_1R_{o2}} - s^2g_{m2}C_c^2 \\ & - \frac{s^2C_c^2 - s^3R_{o2}C_{o2}C_c^2}{R_{o2}} - \frac{sC_c^2}{L_1} + s^2g_{m2}C_1C_c + \frac{s^2C_1C_c + s^3R_{o2}C_{o2}C_cC_1}{R_{o2}} \\ & + \frac{sC_cC_1}{L_1} + \frac{g_{m2}C_c}{L_1} + \frac{C_c + sR_{o2}C_{o2}C_c}{L_1R_{o2}} + s^2C_c^2g_{m2} + \frac{s^2C_c^2 + s^3R_{o2}C_{o2}C_c^2}{R_{o2}} + \frac{sC_c^2}{L_1} \end{aligned} \right]$$

$$+ \frac{1}{sL_1} \left[\begin{aligned} & \left(\frac{-C_cg_{m2}}{L_1} \right) - \frac{C_c + sR_{o2}C_{o2}C_c}{L_1R_{o2}} - \frac{C_c}{sL_1^2} - \frac{g_{m2}C_1}{L_1} + \frac{C_1 + sR_{o2}C_{o2}C_1}{L_1R_{o2}} + \frac{C_1}{sL_1^2} \\ & + \frac{g_{m2}}{s^2L_1^2} + \frac{(1 + sR_{o2}C_{o2})}{s^2L_1^2R_{o2}} \end{aligned} \right]$$

$$\left(\frac{1}{R_{o2}} + sC_{o1} + \frac{1}{sL_1} \right) \left[\begin{aligned} & \frac{2g_{m2}C_c}{L_1} + \frac{2(C_c + sR_{o2}C_{o2}C_c)}{L_1R_{o2}} + \frac{C_c}{sL_1^2} - \frac{C_1}{sL_1^2} - \frac{g_{m2}}{s^2L_1^2} \\ & - \frac{1 - sR_{o2}C_{o2}}{s^2L_1^2R_{o2}} + s^2g_{m2}C_1^2 + \frac{s^2C_1^2 + s^3R_{o2}C_{o2}C_1^2}{R_{o2}} + \frac{sC_1^2}{L_1} \end{aligned} \right] \\ + \left[\begin{aligned} & - \frac{C_cg_{m2}}{sL_1^2} - \frac{C_c - sR_{o2}C_{o2}C_c}{sL_1^2R_{o2}} - \frac{C_c}{s^2L_1^3} + \frac{g_{m2}C_1}{sL_1^2} + \frac{C_1 + sR_{o2}C_{o2}C_1}{sL_1^2R_{o2}} + \frac{C_1}{s^2L_1^3} \\ & + \frac{g_{m2}}{s^3L_1^3} + \frac{(1 + sR_{o2}C_{o2})}{s^3L_1^3R_{o2}} \end{aligned} \right]$$

$$\begin{aligned}
& \therefore \frac{2g_{m2}C_c}{L_1R_{o2}} + \frac{2g_{m2}C_cC_{o2}}{L_1} + \frac{2g_{m2}C_c}{sL_1^2} + \frac{2(C_c + sR_{o2}C_{o2}C_c)}{L_1R_{o2}R_{o1}} + \frac{2(sC_{o1}C_c + s^2R_{o2}C_{o2}C_{o1}C_c)}{L_1R_{o2}} \\
& \frac{2(C_c + sR_{o2}C_{o2}C_c)}{sL_1^2R_{o2}} + \frac{C_c}{sL_1^2R_{o1}} + \frac{C_cC_{o1}}{L_1^2} + \frac{C_c}{s^2L_1^3} - \frac{C_1}{sL_1^2R_{o1}} - \frac{C_1C_{o1}}{L_1^2} - \frac{C_1}{s^2L_1^3} - \frac{g_{m2}}{s^2L_1^2R_{o1}} \\
& - \frac{g_{m2}C_{o1}}{sL_1^2} - \frac{g_{m2}}{s^3L_1^3} - \frac{1-sR_{o2}C_{o2}}{s^3L_1^3R_{o2}} - \frac{1-sR_{o2}C_{o2}}{s^2L_1^2R_{o1}R_{o2}} - \frac{sC_{o1} - s^2R_{o2}C_{o2}C_{o1}}{s^2L_1^2R_{o2}} + \frac{s^2g_{m2}C_1^2}{R_{o1}} \\
& + s^3g_{m2}C_1^2C_{o1} + \frac{sg_{m2}C_1^2}{L_1} + \frac{s^2C_1^2 + s^3R_{o2}C_{o2}C_1^2}{R_{o1}R_{o2}} + \frac{sC_1^2}{L_1R_{o1}} + \frac{s^2C_{o1}C_1^2}{L_1} + \frac{C_1^2}{L_1^2} \\
& - \frac{C_cg_{m2}}{sL_1^2} - \frac{C_c - sR_{o2}C_{o2}C_c}{sL_1^2R_{o2}} - \frac{C_c}{s^2L_1^3} + \frac{g_{m2}C_1}{sL_1^2} + \frac{C_1 + sR_{o2}C_{o2}C_1}{sL_1^2R_{o2}} + \frac{C_1}{s^2L_1^3} + \frac{g_{m2}}{s^3L_1^3} + \frac{1+sR_{o2}C_{o2}}{s^3L_1^3R_{o2}}
\end{aligned}$$

Thus calculating the LCM we get

$$\text{LCM} = L_1^2 s^2 R_{o2} R_{o1}$$

$$\begin{aligned}
& 2g_{m2}C_CL_1R_{o2}s^2 + 2g_{m2}C_C C_{o1}L_1R_{o2}R_{o1}s^2 + g_{m2}C_CR_{o2}R_{o1}s + 2C_CL_1s^2 + 2C_C C_{o2}L_1R_{o2}s^3 \\
& + 2C_C C_{o1}L_1R_{o1}s^3 + 2C_C C_{o1}C_{o2}L_1R_{o2}R_{o1}s^4 + C_CR_{o1}s + C_C C_{o2}R_{o2}R_{o1}s^2 + C_CR_{o2}s \\
& + C_C C_{o1}R_{o2}R_{o1}s^2 - C_1R_{o2}s - C_1C_{o1}R_{o2}R_{o1}s^2 - g_{m2}R_{o2} - g_{m2}C_{o1}R_{o2}R_{o1}s - 1 - C_{o1}R_{o2}s \\
& - C_{o1}R_{o1}s - C_{o2}C_{o1}R_{o2}R_{o1}s^2 + g_{m2}C_1^2L_1^2R_{o2}s^4 + g_{m2}C_1^2L_1^2R_{o2}R_{o1}C_{o1}s^5 + g_{m2}C_1^2L_1^2R_{o2}R_{o1}s^3 \\
& C_1^2L_1^2s^4 + C_1^2C_{o2}L_1^2R_{o2}s^4 + g_{m2}C_1^2L_1^2R_{o1}C_{o1}s^5 + C_{o1}C_{o2}C_1^2L_1^2R_{o2}R_{o1}s^6 + C_1^2L_1R_{o1}s^3 \\
& + C_{o2}C_1^2L_1R_{o2}R_{o1}s^4 + C_1^2L_1R_{o2}s^3 + C_{o1}C_1^2L_1R_{o2}R_{o1}s^4 + C_1^2R_{o2}R_{o1}s^2 + g_{m2}C_1R_{o2}R_{o1}s + C_1R_{o1}s + C_{o2}C_1s \\
& + C_{o2}C_1R_{o2}R_{o1}s^2
\end{aligned}

$$L_1^2R_{o2}R_{o1}s^2$$$$

After simplifying the above terms and combining the same power terms together the transfer function is given as,

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m2}C_c \left[L_1^2 s^2 R_{o2} R_{o1} \right]}{|A|}$$

$$\begin{aligned}
& s^7 [C_{o2}C_{o1}R_{o2}R_{o1}C_1^2L_1^4] + s^6 [C_{o2}R_{o2}C_1^2L_1^4 + C_1^2C_{o1}R_{o1}L_1^4 + g_{m2}C_1^2C_{o1}L_1^4R_{o1}R_{o2}] \\
& + s^5 [C_{o2}R_{o2}C_1^2L_1^3R_{o1} + C_{o2}C_1^2R_{o1}R_{o2}L_1^3 + g_{m2}C_1^2L_1^4R_{o2} + 2C_{o1}C_{o2}C_cL_1^3R_{o2}R_{o1} + C_1^2L_1^4] \\
& + s^4 [R_{o2}C_1^2L_1^3 + C_1^2R_{o1}L_1^3 + g_{m2}C_1^2L_1^3R_{o2}R_{o1} + 2C_{o1}C_cL_1^3R_{o1} + 2C_{o2}C_cL_1^3R_{o2}] \\
& + s^3 \left[R_{o2}C_1^2L_1^2R_{o1} - C_{o2}C_{o1}R_{o1}R_{o2}L_1^2 - C_1C_{o1}L_1^2R_{o2}R_{o1} + C_{o1}C_cL_1^2R_{o2}R_{o1} + C_{o2}C_cL_1^2R_{o2}R_{o1} \right. \\
& \left. + 2C_cL_1^3 + 2g_{m2}C_cC_{o1}L_1^3R_{o2}R_{o1} + 2g_{m2}C_cL_1^3R_{o2} + C_1C_{o2}L_1^2R_{o2}R_{o1} \right] \\
& + s^2 \left[R_{o1}C_1L_1^2 + g_{m2}C_1R_{o1}R_{o2}L_1^2 - C_{o1}L_1^2R_{o1} - C_{o1}L_1^2R_{o2} - g_{m2}C_1L_1^2R_{o2}R_{o1} \right. \\
& \left. - C_1L_1^2R_{o2} + C_cL_1^2R_{o2} + C_cL_1^2R_{o1} + g_{m2}C_cL_1^2R_{o2}R_{o1} \right] \\
& + s [-g_{m2}L_1^2R_{o2} - L_1^2]
\end{aligned}$$

After putting the typical values of the transconductance, the output resistance, the output capacitance for the first stage and the second stage respectively, the higher order terms were eliminated and the transfer function of a much simplified form was obtained. The transfer function with three poles and two zero is obtained.

Appendix B

TSMC 0.25 μ m Process Parameters

simulator lang=spectre

TSMC SPICE MODEL

PROCESS : 0.25um Mixed-Signal SALICIDE(2P5M or 1P5M+, 2.5V/3.3V)

MODEL : BSIM3 (Mixed V3.1 & V3.2)

DOC. NO.: T-025-MM-SP-001

VERSION : 1.6

SPECTRE VERSION : V4.4.5

IN THIS MODEL LIB CONTAINS :

1.LIB TT

SS

FF

SF

FS

(2.5V Nominal Vt devices with different geometric and corner models)

1)To use these models directly by programming in this style:

include "lib_path/lib_name" section=tt

EX: .lib '/home/user/tsmc/MIXED025/mix025_1.l' TT

for typical 2.5V Nominal Vt Devices

.lib '/home/user/tsmc/MIXED025/mix025_1.l' TT_3V

corner_name

TT : typical model for 2.5V Nominal Vt devices

SS : Slow NMOS Slow PMOS model for 2.5V Nominal Vt devices

FF : Fast NMOS Fast PMOS model for 2.5V Nominal Vt devices

SF : Slow NMOS Fast PMOS model for 2.5V Nominal Vt devices

FS : Fast NMOS Slow PMOS model for 2.5V Nominal Vt devices

2)HDIF depends on your layout poly spacer to contact center distance.

The value listed here is TSMC minimum-rule value. you can change it according to your layout.

2.5V NOMINAL Vt DEVICES LIB

CORNER_LIB OF TYPICAL MODEL

library tsmclib

section tt

parameters toxp=5.4e-9

parameters toxn=5.4e-9

parameters dxi=0

```
parameters dxw=0
parameters dvthn=0.0
parameters dvthp=0.00
parameters cjn=1.836615e-03
parameters cjp=1.833935e-03
parameters cjswn=4.234822e-10
parameters cjswp=3.472876e-10
parameters cgon=1.3e-10
parameters cgop=1.6e-10
parameters cgln=2.1e-10
parameters cglp=2.1e-10
parameters cjgaten=3.286035e-10
parameters cjgatep=2.500235e-10
parameters hdifn=2.625e-07
parameters hdifp=2.625e-7
include "mix025_1.scs" section=mos
endsection tt
```

```
//          NORMAL DEVICES MODEL

//

// *****

// *****

//          NMOS DEVICES MODEL

// *****

model nch bsim3v3 {

    1: type=n minr=1e-60 lmin=1.2e-06 - dxi lmax=2.1e-05 wmin=1.2e-06
    - dxw wmax=1.01e-04 tnom=25 xl=3e-08 + dxi flkmod=1 af=0.8824 kf=3.454e-
    24 xw=0 dxw version=3.2 tox=toxn xj=1e-07 nch=1.63e+17 lln=1 lwn=1 wln=1
    wwn=1 lint=2e-08 wint=2e-08 mobmod=1 binunit=2 dwg=0 dwb=0
    vth0=0.4767749 + dvthn lvth0=3.507137e-08 + wvth0=-1.453229e-08 pvth0=-
    6.620086e-15 k1=0.4472964 lk1=-5.39693e-08 wk1=-4.269873e-08 +
    pk1=5.981896e-14 k2=0.004538423 lk2=2.041006e-08 wk2=1.682965e-08
    pk2=-2.784819e-14 + k3=0 dvt0=0 dvt1=0 dvt2=0 dvt0w=0 dvt1w=0 dvt2w=0
    nlx=0 w0=0 k3b=0 vsat=120633 + lvsat=-0.01265326 ua=-9.218065e-10 lua=-
    1.161761e-16 wua=1.451009e-16 pua=-5.566174e-23 + ub=1.81497e-18
    lub=1.561614e-25 wub=-2.338524e-25 pub=8.58042e-33 uc=4.365745e-11 +
    luc=8.007525e-18 wuc=-7.436576e-18 puc=-6.149303e-24 rdsw=187 prwb=0
    prwg=0 wr=1 + u0=0.03077917 lu0=5.598957e-11 wu0=-8.158919e-11
    pu0=1.090017e-15 a0=0.5252816 + la0=4.042826e-08 wa0=1.225374e-07
    pa0=-2.063631e-13 keta=0.003461425 lketa=-9.223886e-09 + wketa=-
```

8.366612e-11 pketa=1.672486e-15 a1=0 a2=0.65 ags=0.01 b0=0 b1=0 voff=-
 0.1517445 + lvoff=2.086556e-08 wvoff=6.482217e-09 pvoff=-7.791971e-15
 nfactor=1 cit=0.000377699 + lcit=7.405382e-10 wcit=-6.34899e-10
 pcit=7.555298e-16 cdsc=0 cdscb=0 cdsd=0 eta0=3.836953e-05 +
 leta0=2.324929e-10 weta0=8.055062e-12 peta0=-1.610206e-16 etab=-
 4.68351e-05 letab=-6.326623e-11 + dsub=0 pclm=0.4755805 lpclm=4.88145e-
 07 wpclm=-6.231367e-09 ppclm=1.245653e-13 + pdiblc1=1e-05
 pdiblc2=0.0002151594 lpdiblc2=5.69396e-09 pdiblc3=0.01 drout=0
 pscbe1=1.213673e+08 + lpscbe1=265.5531 wpscbe1=-3.167115 ppscbe1=-
 1.324478e-05 pscbe2=1e-06 pvag=0 delta=0.01 + alpha0=0 beta0=20.54463
 kt1=-0.2402984 lkt1=-1.511487e-08 wkt1=1.116811e-08 pkt1=-1.329005e-14 +
 kt2=-0.02232689 lkt2=-1.527194e-08 wkt2=-1.12105e-08 pkt2=1.287179e-14
 at=35000 + ute=-1.688541 lute=3.778586e-09 wute=1.029916e-07 pute=-
 5.895606e-14 ua1=9.999999e-11 + ub1=0 uc1=-4.534566e-11 luc1=7.638851e-
 17 wuc1=8.059368e-17 puc1=-8.934457e-23
 + kt1l=0 prt=0 cj=cjn mj=0.4708251 pb=0.9597901 cjsw=cjsw n cjsw=0.379613
 pbsw=0.9597901 + cjswg=cjgaten mjswg=0.379613 pbswg=0.9597901
 tcj=0.0007391288 tcjsw=0.0009081566 + tpb=0.001293296 tpbsw=0.001178533
 js=2e-06 jsw=5e-10 cgdo=cgon cgso=cgon capmod=3 + nqsmod=0 xpart=1 cf=0
 tlev=1 tlevc=1 xti=3 n=1 hdif=hdifn ldif=1.2e-07 rsh=4.5 + rs=0 rd=0 dlc=3.49e-9
 dwc=5.76e-10 clc=3.82e-08 cle=0.6972 acde=0.4 moin=10+ noff=1.4959

voffcv=-0.074 ckappa=2.8769 cgdI=cgln cgsl=cgln cgbo=1e-13 toxm=5.4e-9 +
tcjswg=0.0009081566 tpbswg=0.001178533 alpha1=18.2625

```
// *****
```

```
//          PMOS DEVICES MODEL          *
```

```
// *****
```

```
}
```

```
model pch bsim3v3 {
```

```
1: type=p minr=1e-60 lmin=1.2e-06 - dxi lmax=2.1e-05 wmin=1.2e-06
```

```
+ - dxw wmax=1.01e-4 tnom=25 version=3.2 flkmod=1 af=1.2828 kf=1.184e-23
```

```
tox=toxp + xj=1e-07 nch=4.15e+17 lln=1 lwn=1 wln=1 wwn=1 lint=5.2e-08 ll=0
```

```
lw=0 lwl=0 wint=2.5e-08 + wl=0 ww=0 wwl=0 mobmod=1 binunit=2 xl=3e-08 +
```

```
dxi xw=0 + dxw dwg=0 dwb=0 vth0= + - 0.5964869 + dvthp lvth0=-1.227094e-08
```

```
wvth0=5.331006e-09 pvth0=4.951822e-15 + k1=0.6000811 lk1=-4.272914e-08
```

```
wk1=-1.275793e-08 pk1=6.864224e-14 k2=0.005330595 + lk2=1.236721e-08
```

```
wk2=4.946015e-09 pk2=-2.049107e-14 k3=0 dvt0=0 dvt1=0 dvt2=0 + dvt0w=0
```

```
dvt1w=0 dvt2w=0 nlx=0 w0=0 k3b=0 vsat=180000 ua=6.278216e-10 lua=-
```

```
7.532845e-17 + wua=1.063208e-16 pua=3.038439e-23 ub=5.036719e-19
```

```
lub=2.151329e-25 wub=-2.467893e-25 + pub=-3.285619e-32 uc=-5.793595e-11
```

```
luc=2.487329e-17 wuc=-3.885884e-17 puc=4.396424e-24 + rdsw=1000 prwb=0
```

```
prwg=0 wr=1 u0=0.009563554 lu0=-4.400553e-10 wu0=3.135935e-10 + pu0=-
```

2.203534e-16 a0=0.7584345 la0=-1.058737e-07 wa0=4.878771e-08 pa0=-
 2.4806e-14 + keta=0.02091301 lketa=-2.785713e-08 wketa=-2.911637e-09
 pketa=1.548454e-14 a1=0 + a2=0.9 ags=0.01 b0=0 b1=0 voff=-0.1337011
 lvoff=2.374397e-09 wvoff=-3.594663e-09 + pvoff=1.62976e-14 nfactor=1 cit=-
 0.0001159413 lcit=3.176463e-10 wcit=8.992995e-12 + pcit=-1.791944e-16
 cdsc=0 cdsb=0 cdsd=0 eta0=5e-05 etab=-5e-05 dsub=0 pclm=0.5726337 +
 lpclm=6.965759e-07 wpclm=-1.384238e-07 ppclm=2.927752e-13 pdiblc1=1e-05
 pdiblc2=0.005 + pdiblc3=0.01 drout=0 pscbe1=5e+08 pscbe2=1e-06 pvag=0
 delta=0.01 alpha0=0 beta0=19.43759 + kt1=-0.2497616 lkt1=-5.655294e-09
 wkt1=1.055803e-08 pkt1=-3.103606e-15 kt2=-0.02983099 + lkt2=-5.4268e-10
 wkt2=1.542839e-09 pkt2=-2.182701e-15 at=10000 ute=-1.037682
 lute=9.182398e-08 + wute=6.781937e-09 pute=-6.661502e-15 ua1=9.999999e-
 11 ub1=0 uc1=3.832679e-11 luc1=1.703325e-17 + wuc1=6.655088e-17 puc1=-
 3.097963e-23 kt1l=0 prt=0 hdif=hdifp ldif=1.2e-07 + rsh=3.5 rs=0 rd=0 cj=cjp
 mj=0.4746122 pb=0.9522272 cjsw=cjswp mjsw=0.3296904 pbsw=0.9522272 +
 cjswg=cjgatep mjswg=0.3296904 pbswg=0.9522272 tcj=0.0008154354
 tcjsw=0.0006079875 + tpb=0.00140666 tpbsw=0.001610754 cgdo=cgop
 cgso=cgop capmod=3 nqsmod=0 xti=3 n=1 + xpart=1 cf=0 tlev=1 tlevc=1 js=7e-
 07 jsw=1.4e-10 dlc=4.53e-8 dwc=2.51e-9 clc=6.60e-08 + cle=4.25 acde=1.54
 moin=23 noff=1.855 voffcv=-0.09 ckappa=1.1056 cgbo=1e-13 cgdl=cglp +
 cgsl=cglp toxm=5.4e-9 tcjswg=0.0006079875 tpbswg=0.001610754
 alpha1=0.46878

Chip Layout

